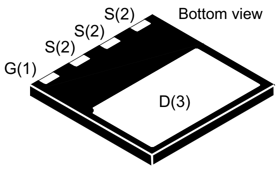
STL18NM60N

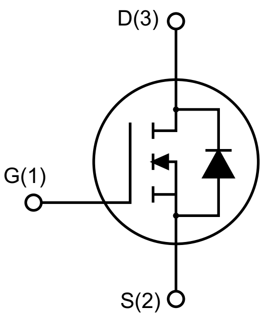
N-channel 600 V, 0.26 Ω typ., 12 A MDmesh™ II Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STL18NM60N	650 V	0.310 Ω	12 A (1)

1. The value is rated according to $R_{thj\text{-}case}$

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STL18NM60N	18NM60N	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	12	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	7.5	A
I_D(2)	Drain current (continuous) at T_{amb} = 25 °C	2.1	A
I_D(2)	Drain current (continuous) at T_{amb} = 100 °C	1.2	A
I_{DM}(2),(3)	Drain current (pulsed)	8.4	A
P_{TOT} (2)	Total dissipation at T_{amb} = 25 °C	3	W
P_{TOT}(1)	Total dissipation at T_C = 25 °C	110	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	350	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj\text{-}case}$
2. When mounted on 1inch² FR-4 board, 2 oz Cu
3. Pulse width limited by safe operating area
4. $I_{SD} \leq$ 12 A, di/dt $\leq$ 400 A/µs, $V_{DSpeak} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.14	°C/W
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-amb max	42	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V			1	µA
		V_{DS} = 600 V, T_C= 125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 6 A		0.260	0.310	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1000	-	pF
C_{oss}	Output capacitance			60	-	pF
C_{rss}	Reverse transfer capacitance			3	-	pF
$C_{oss\ eq.}$ (1)	Output equivalent capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	225	-	pF
R_G	Intrinsic gate resistance	f = 1, I_D=0	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 12 A, V_{GS} = 10 V (see *Figure 14*)	-	35	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*)	-	12	-	ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turn-on delay time			55		ns
t_f	Fall time			25		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM} (1)	Source-drain current (pulsed)		-		48	A
V_{SD} (2)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 15*)	-	300		ns
Q_{rr}	Reverse recovery charge		-	4.0		µC
I_{RRM}	Reverse recovery current		-	25		A
t_{rr}	Reverse recovery time	V_{DD} = 60 V di/dt = 100 A/µs, I_{SD} = 12 A T_j=150 °C (see *Figure 15*)	-	360		ns
Q_{rr}	Reverse recovery charge		-	4.5		µC
I_{RRM}	Reverse recovery current		-	25		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

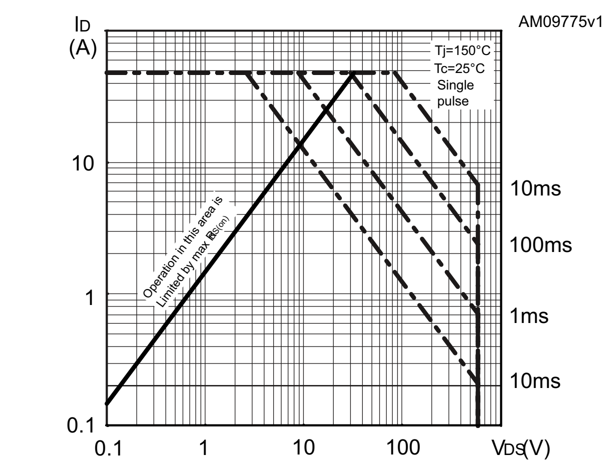


Figure 3. Thermal impedance

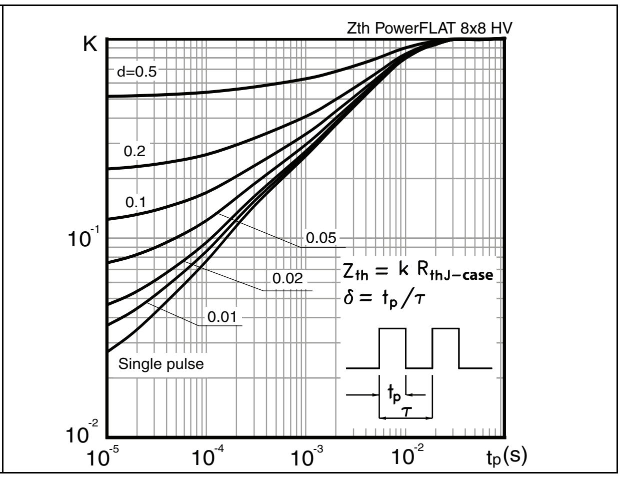


Figure 4. Output characteristics

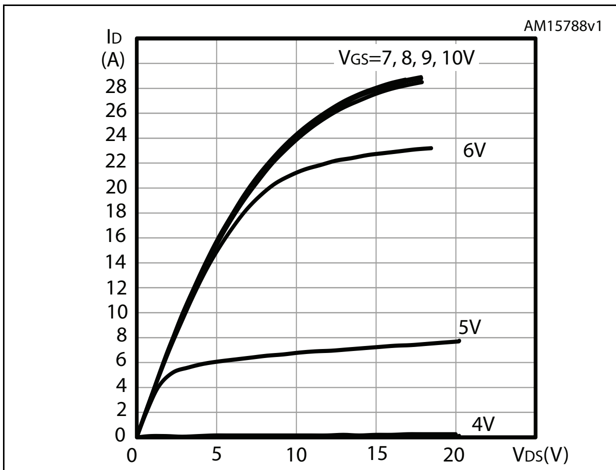


Figure 5. Transfer characteristics

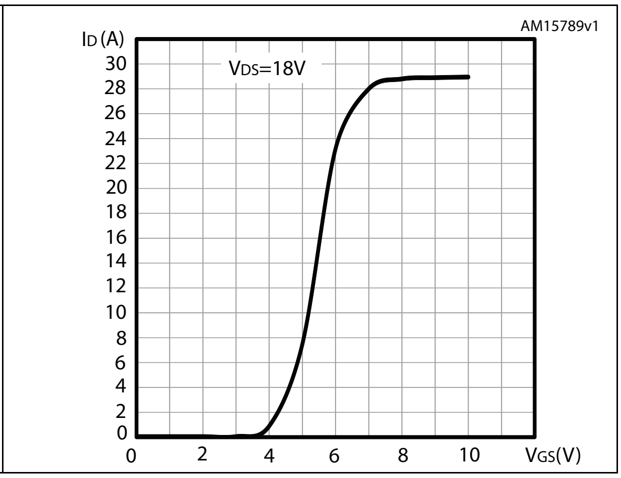


Figure 6. Normalized V_{DS} vs temperature

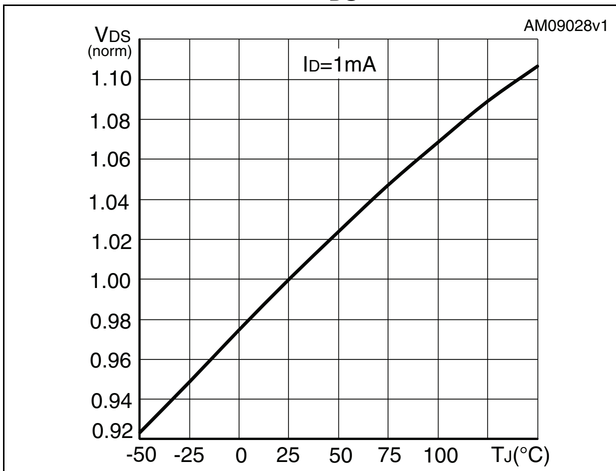


Figure 7. Static drain-source on-resistance

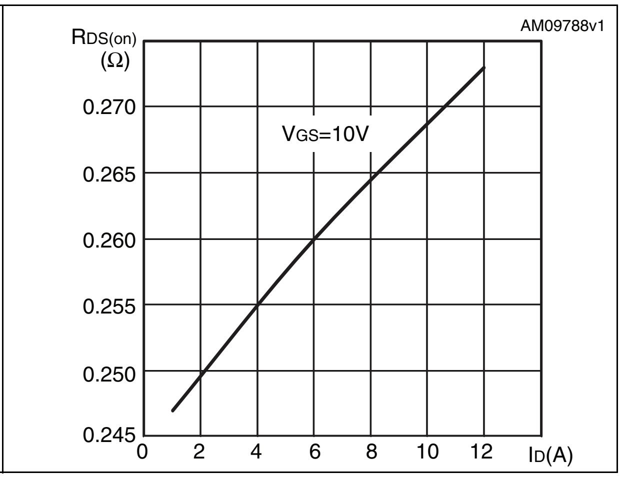


Figure 8. Gate charge vs gate-source voltage

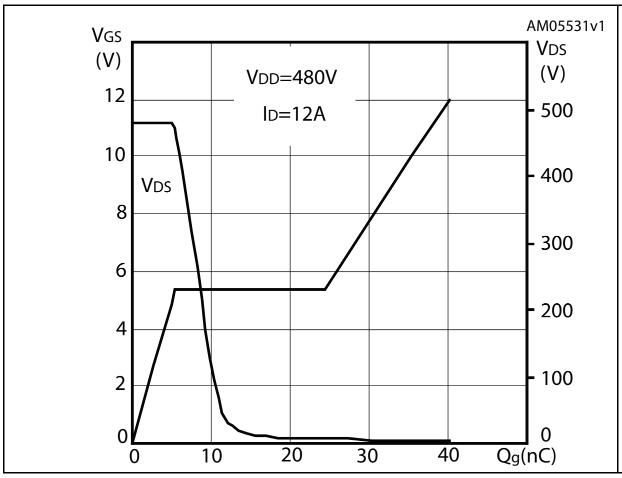


Figure 9. Capacitance variations

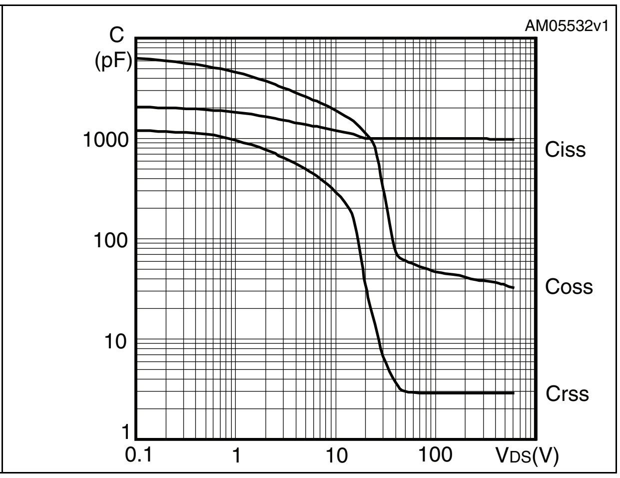


Figure 10. Normalized gate threshold voltage vs temperature

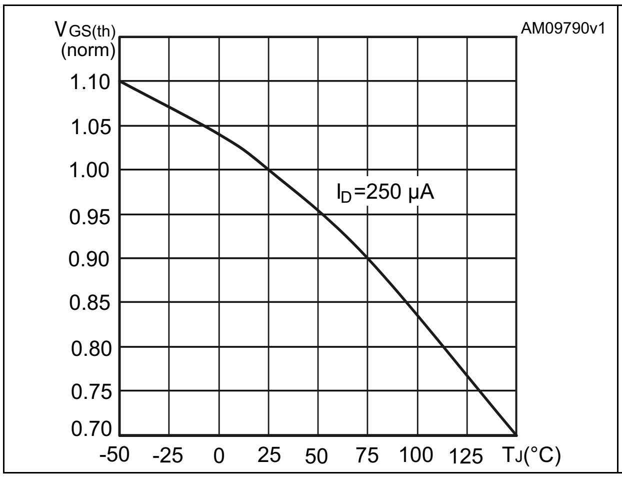


Figure 11. Normalized on-resistance vs temperature

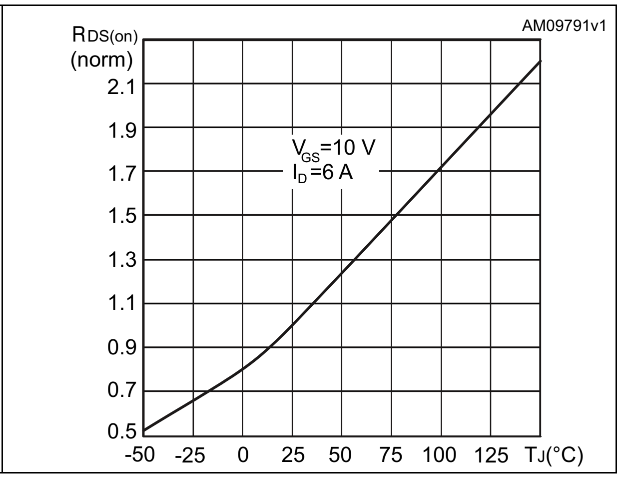
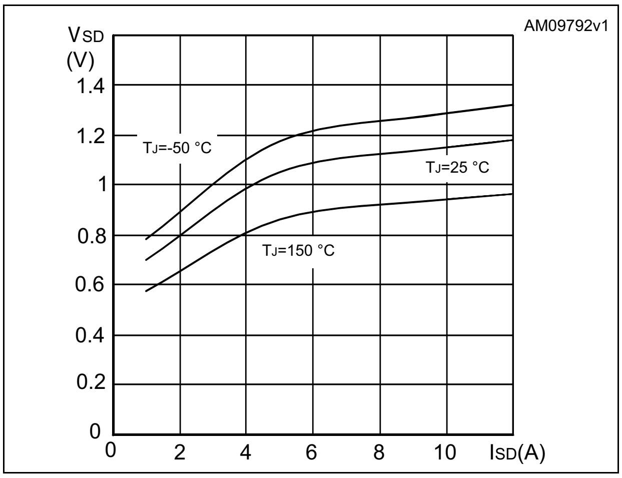


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

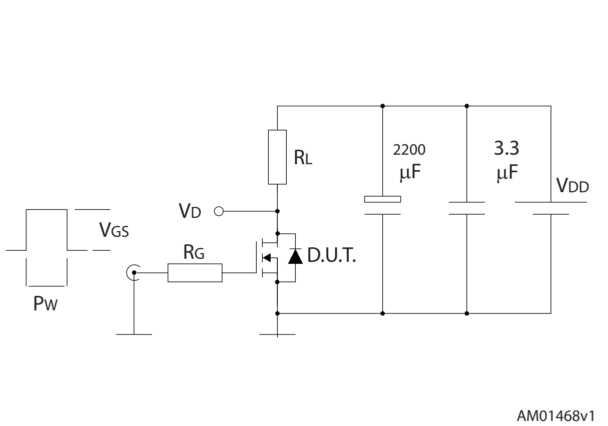


Figure 14. Gate charge test circuit

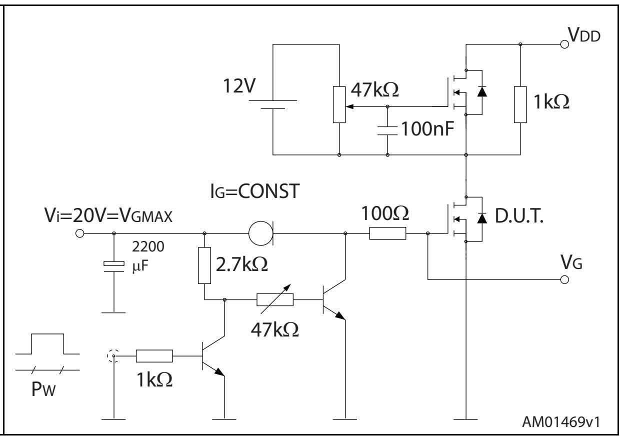


Figure 15. Test circuit for inductive load switching and diode recovery times

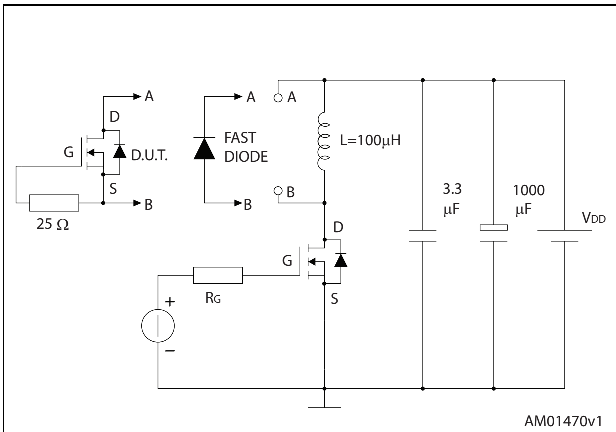


Figure 16. Unclamped inductive load test circuit

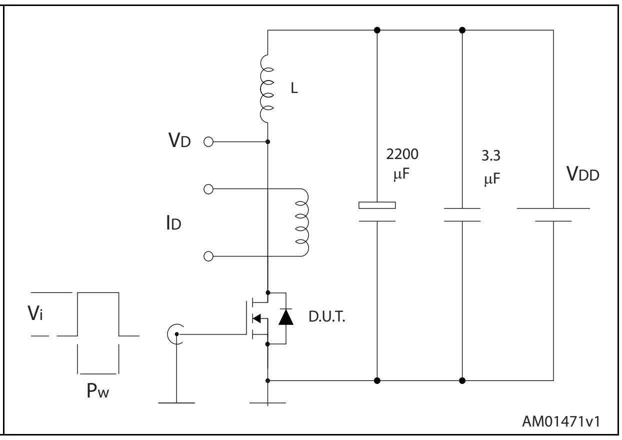


Figure 17. Unclamped inductive waveform

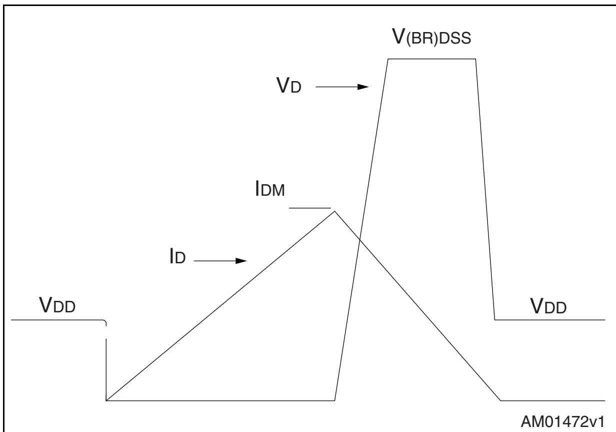
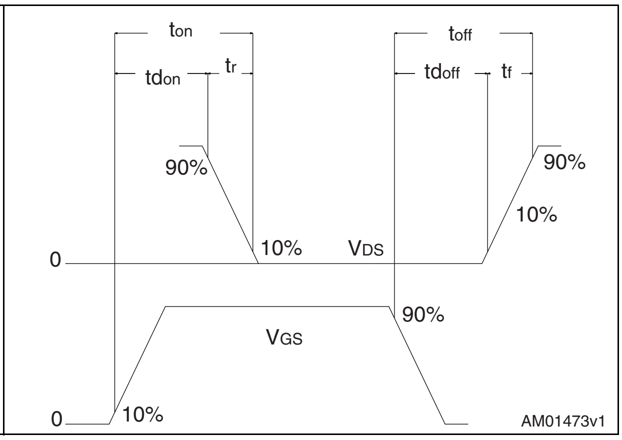


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 19. PowerFLAT™ 8x8 HV drawing mechanical data

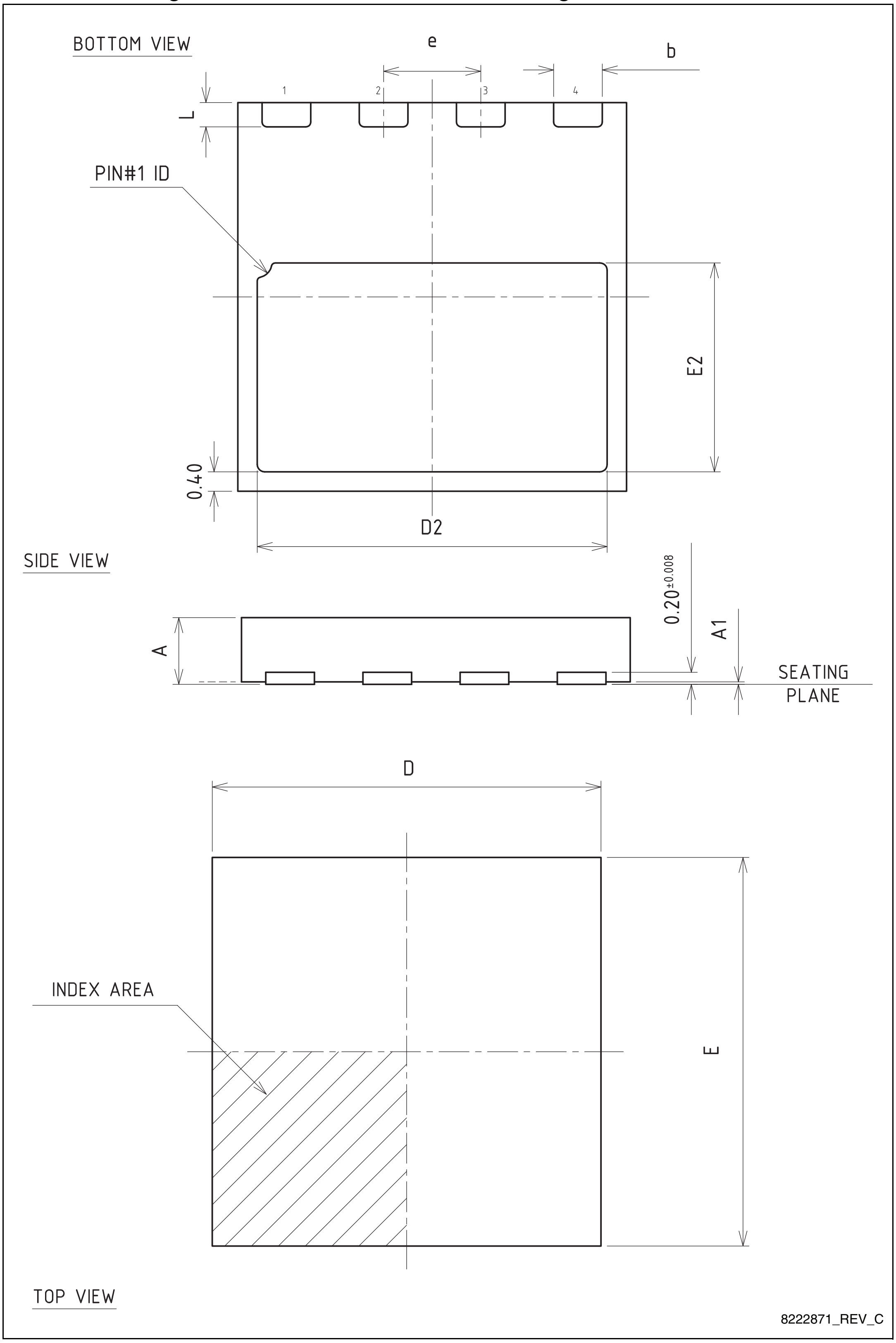
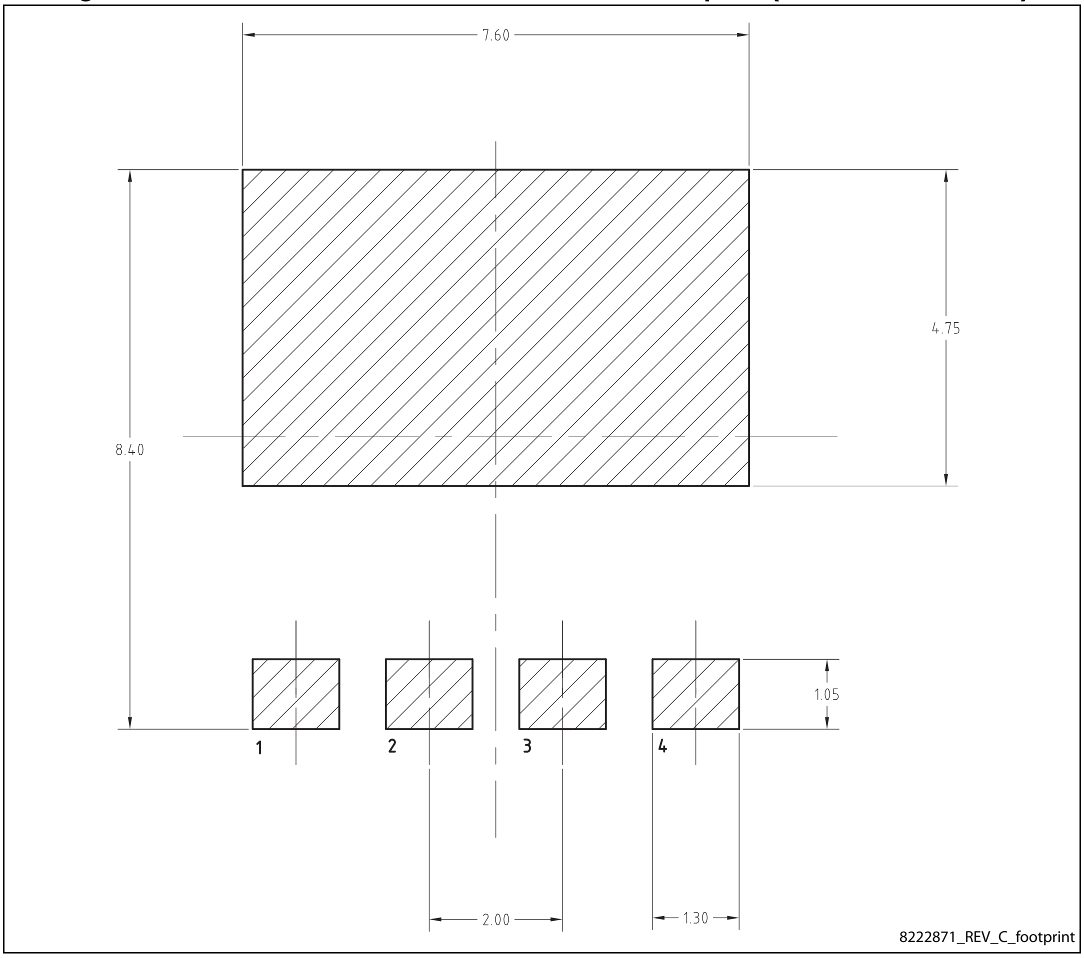


Figure 20. PowerFLAT™ 8x8 HV recommended footprint (dimensions in mm.)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 8x8 HV tape

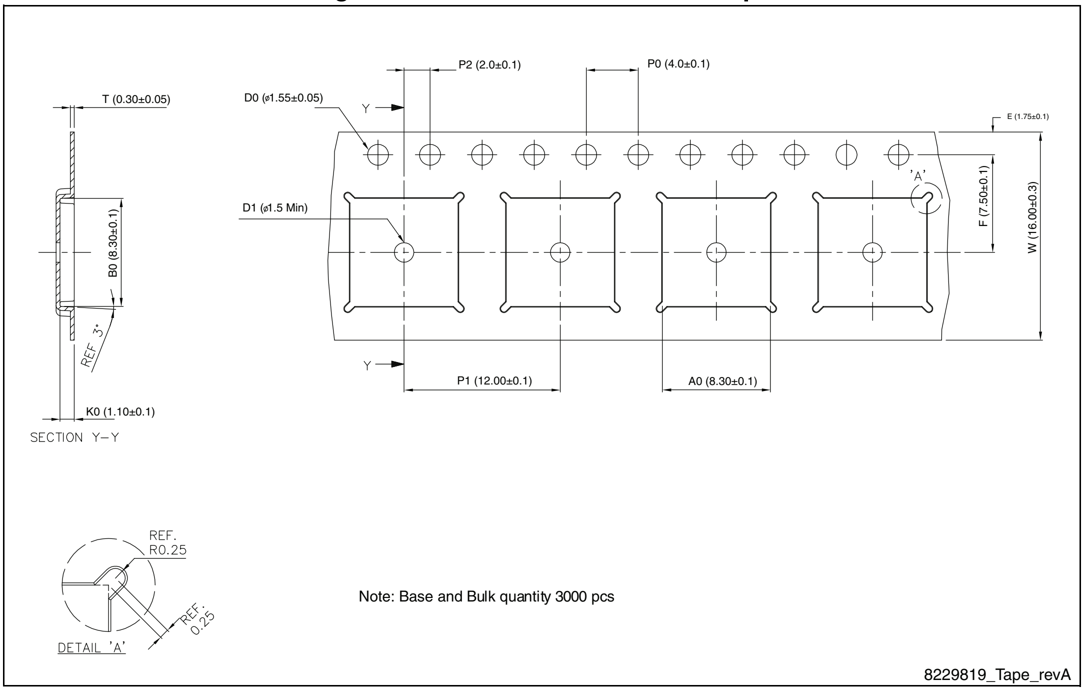


Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape.

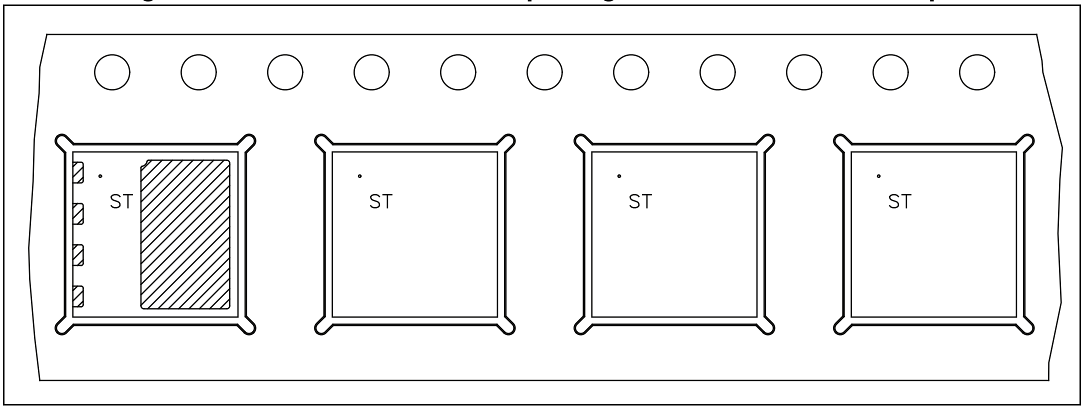
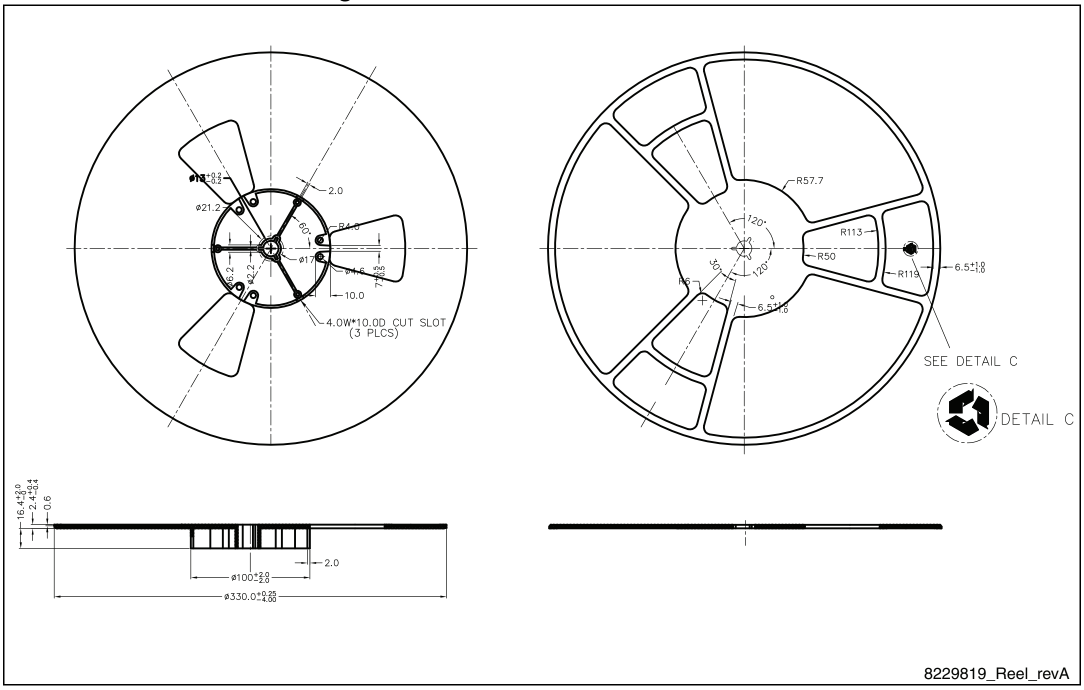


Figure 23. PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-May-2011	1	First release.
03-Nov-2011	2	*Section 4: Package mechanical data* has been updated. Minor text changes.
28-Nov-2013	3	– Modified: title – Modified: V_{GS}, I_{AR}, E_{AS} values in *Table 2* – Modified: note 2 in *Table 2* – Modified: $R_{thj\text{-}amb}$ value in *Table 3* – Modified: I_D value in *Table 5* – Modified: the entire typical value in *Table 6* – Modified: I_{SD} value in *Table 6* – Modified: *Figure 3*, *4*, *5*, *13*, *14*, *15*, and *16* – Updated: *Section 4: Package mechanical data* and added *Section 5: Packaging mechanical data*