1/4-Inch VGA Digital Image Sensor

MT9V011 Data Sheet

For the latest data sheet revision, please refer to Aptina's Web site: www.aptina.com

Features

- Ultra low-power, low cost CMOS image sensor
- Superior low-light performance
- Simple two-wire serial interface
- Auto black level calibration
- Window Size: VGA, programmable to any smaller format (QVGA, CIF)
- Programmable Controls: Gain, frame rate, left-right and top-bottom image reversal, window size, and panning

Applications

- Cellular phones
- PDAs
- PC Cameras
- Toys and other battery-powered products

Ordering Information

Table 1: Available Part Numbers

Part Number	Description
MT9V011P11STC:B	28-Pin PLCC
MT9V011DO0STCC82SC1	Die

Table 2: Key Performance Parameters

Parameter		Value
Optical format		1/4-inch (4:3)
Active imager size		3.58mm(H) x 2.69mm(V), 4.48mm Diagonal
Active pixels		640H x 480V
Pixel size		5.6µm x 5.6µm
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ master clock		13.5 MPS/27 MHz
Frame rate	VGA (640 x 480)	30 fps at 27 MHz
	CIF (352 x 288)	Programmable up to 60 fps
	QVGA (320 x 240)	Programmable up to 90 fps
ADC resolution		10-bit, on-chip
Responsivity		2.0 V/lux-sec (550nm)
Dynamic range		60dB
SNR_{MAX}		45dB
Supply voltage		2.8V ±0.25V
Power consumption		70mW at 2.8V, 27 MHz, 30 fps
Operating temperature		–20°C to +60°C
Packaging		28-Pin PLCC

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General Description

The Aptina™MT9V011 is a 1/4-inch VGA-format CMOS active-pixel digital image sensor. The active imaging pixel array is 649H x 489V. It incorporates sophisticated camera functions on-chip such as windowing, column and row mirroring. It is programmable through a simple two-wire serial bus interface and has very low power consumption.

The MT9V011 features Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a VGA-size image at 30 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock which is synchronous with valid data.

Figure 1: Block Diagram

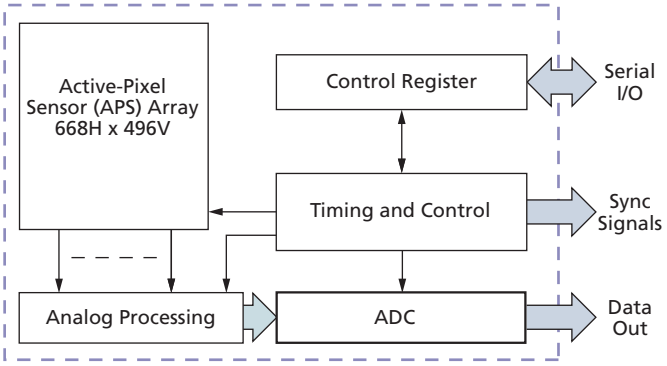
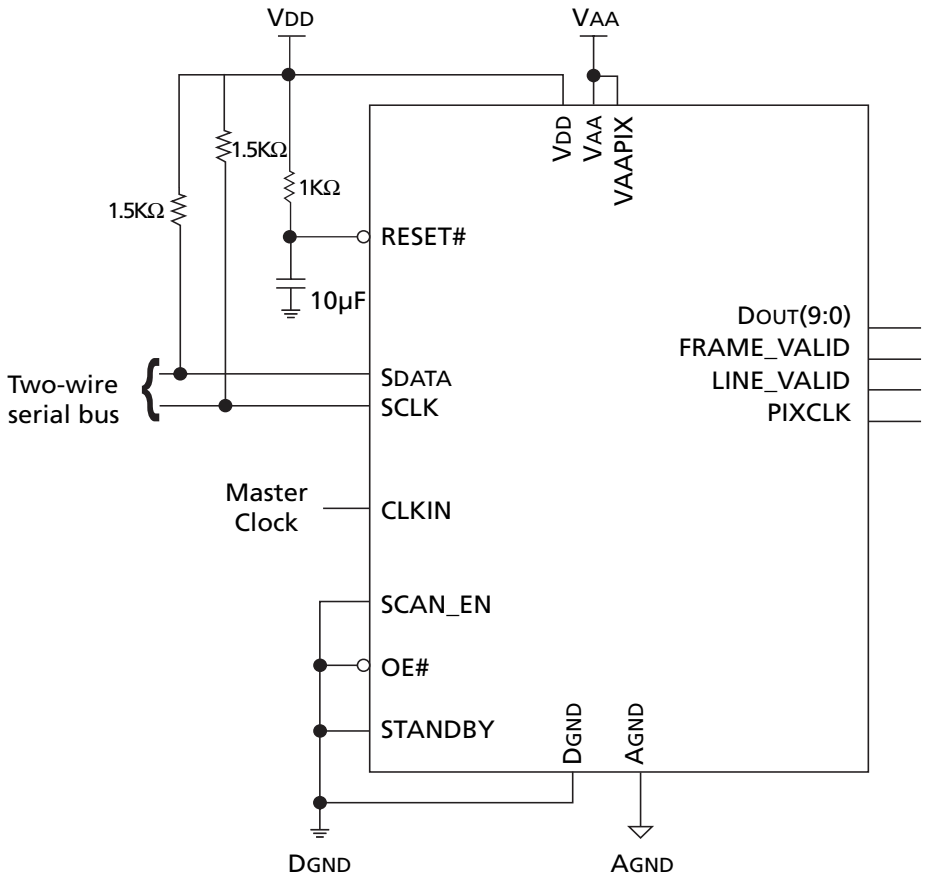


Figure 2: Typical Configuration (Connection)



Note: 1.5KΩ resistor value is recommended, but may be higher for slower two-wire speed.

Figure 3: 28-Pinout Diagram

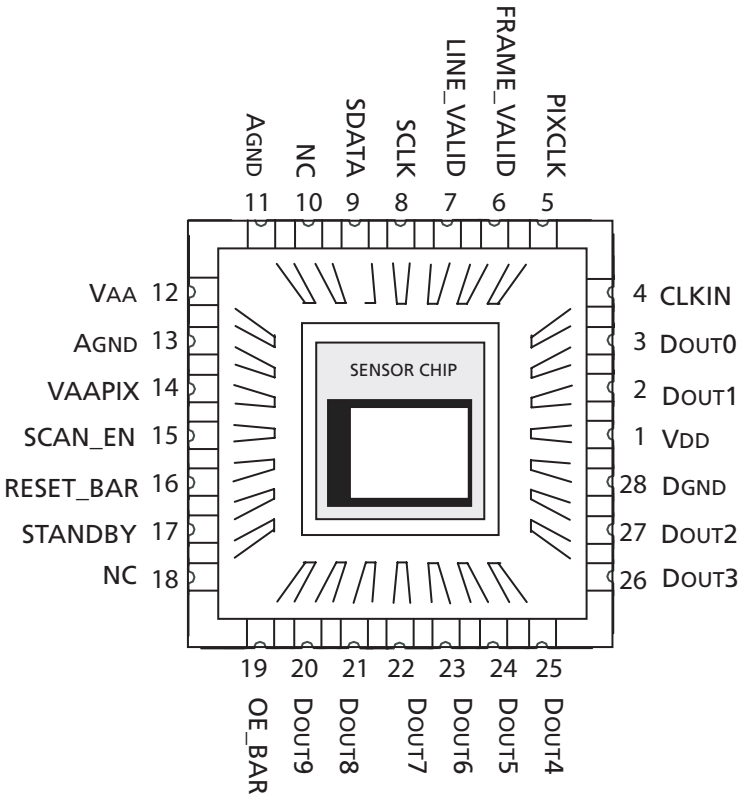


Table 2: Pin Description

Pin Number	Name	Type	Description
12	VAA	Power	Analog Power (2.8V).
14	VAAPIX	Power	Pixel Power (2.8V).
1	VDD	Power	Digital Power Supply (2.8V).
28	DGND	Ground	Digital Ground.
11, 13	AGND	Ground	Analog Ground.
14	CLKIN	Input	Master Clock into sensor (27 MHz maximum).
19	OE_BAR	Input	Output_Enable_Bar pin. When HIGH: disables the pixel data output drivers.
16	RESET_BAR	Input	Asynchronous reset of sensor when LOW. All registers assume factory defaults.
15	SCAN_EN	Input	Tie to Digital Ground.
8	SCLK	Input	Serial Clock.
17	STANDBY	Input	When HIGH: disables the imager.
9	SDATA	Bidirectional	Serial Data I/O.
3	DOUT0	Output	Pixel Data Output Bit 0, D0 (LSB).
2	DOUT1	Output	Pixel Data Output Bit 1, D1.
27	DOUT2	Output	Pixel Data Output Bit 2, D2.
26	DOUT3	Output	Pixel Data Output Bit 3, D3.
25	DOUT4	Output	Pixel Data Output Bit 4, D4.
24	DOUT5	Output	Pixel Data Output Bit 5, D5.
23	DOUT6	Output	Pixel Data Output Bit 6, D6.

Table 2: Pin Description (continued)

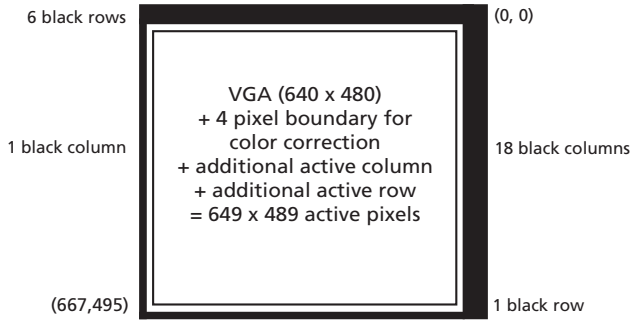
Pin Number	Name	Type	Description
22	DOUT7	Output	Pixel Data Output Bit 7, D7.
21	DOUT8	Output	Pixel Data Output Bit 8, D8.
20	DOUT9	Output	Pixel Data Output Bit 9, D9 (MSB).
6	FRAME_VALID	Output	Active HIGH during frame of valid pixel data.
7	LINE_VALID	Output	Active HIGH during line of selectable valid pixel data (see Reg0x20 for options).
5	PIXCLK	Output	Pixel Clock Output. Pixel data outputs are valid during rising edge of this clock. Frequency = 1/2 (master clock).
10, 18	NC	—	No connect.

Pixel Data Format

Pixel Array Structure

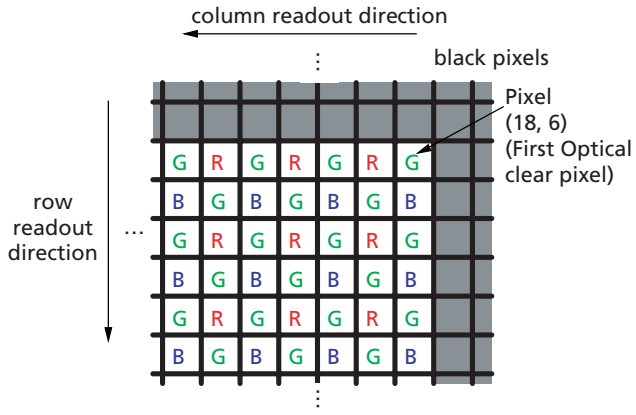
The MT9V011's pixel array is 668 columns by 496 rows. The first 18 columns and the first 6 rows of pixels are optically black and can be used to monitor the black level. The last column and the last row of pixels are also optically black. The black row data is used internally for automatic black level adjustment. There are 649 columns by 489 rows of optically active pixels, which provides a four-pixel boundary around the VGA (640 x 480) image to avoid boundary affects during color interpolation and correction. The additional active column and additional active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel, as shown in Figure 4.

Figure 4: Pixel Array Description



The MT9V011 uses the RGB Bayer color pattern. Even numbered rows contain green and red color pixels, and odd numbered rows contain blue and green color pixels. Likewise, even numbered columns contain green and blue color pixels, and odd numbered columns contain red and green color pixels.

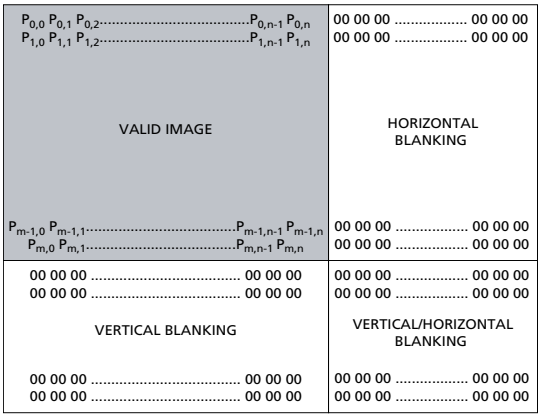
Figure 5: Pixel Color Pattern Detail (Top Right Corner



Output Data Format

The MT9V011 image data is read-out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 6. The amount of horizontal and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. See "Output Data Timing" on page 11 for the description of FRAME_VALID timing.

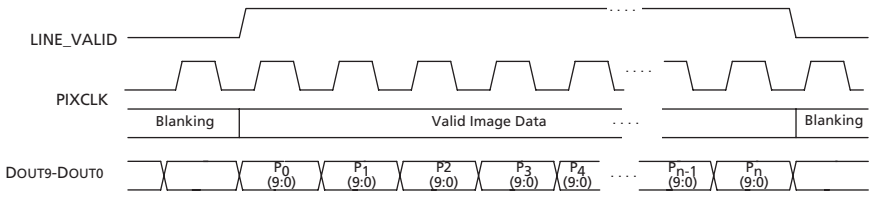
Figure 6: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9V011 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

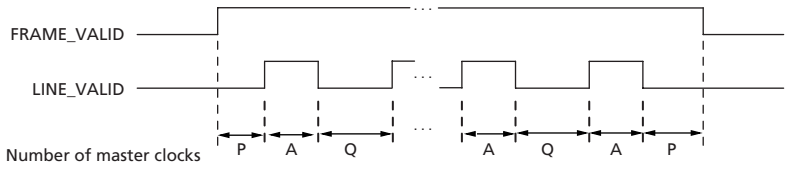
Figure 7: Timing Example of Pixel Data



The rising edges of the PIXCLK signal are nominally timed to occur one-half of a master clock period after the DOUT edges. This allows PIXCLK to be used as a clock to latch the data. The PIXCLK is HIGH for one complete master clock period and then LOW for one complete master clock period. It is continuously enabled, even during the blanking period. The MT9V011 can be programmed to move the PIXCLK edge relative to the DOUT transitions from +1 to -1 master clock, in steps of one-half of a master clock. This can be achieved by programming the corresponding bits in Reg0x07.

The parameters P, A, and Q in Figure 8 are defined in Table 3.

Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals



Frame Timing Formulas

Table 3: Frame Time

Parameter	Name	Equation	Default Timing At 27 MHz
A	Active Data Time	(Reg0x04 + 1) x (Reg0x0A + 2)	640 pixel clocks = 1280 master = 47.4µs
P	Frame Start/End Blanking	6 x (Reg0x0A + 2)	6 pixel clocks = 12 master = 0.44µs
Q	Horizontal Blanking	(113 + Reg0x05) x (Reg0x0A + 2) (minimum Reg0x05 value = 9)	244 pixel clocks = 488 master = 18.07µs
A+Q	Row Time	(Reg0x04 + 1 + 113 + Reg0x05) x (Reg0x0A + 2)	884 pixel clocks = 1,768 master = 65.48µs
V	Vertical Blanking	(Reg0x06 + 1) x (A + Q) + (Q - 2 x P)	25,868 pixel clocks = 51,736 master = 1.92µs
N_{rows} x (A + Q)	Frame Valid Time	(Reg0x03 + 1) x (A + Q) - (Q - 2 x P)	424,088 pixel clocks = 848,176 master = 31.41µs
F	Total Frame Time	(Reg0x03 + 1 + Reg0x06 + 1) x (A + Q)	449,956 pixel clocks = 899,912 master = 33.33µs

The constant 113 in the formulas in Table 3 is the constant value in default mode, when 8 dark columns are read out through Reg0x30. The constant follows the dark columns read out as shown in Table 4.

Sensor timing is shown above in terms of pixel clock and master clock cycles (please refer to Figure 7). The recommended master clock frequency is 27 MHz.

Table 4: Constant Value

Reg 0x30, bit 1:0	Constant	
1x	121	For 16 columns
01	113	For 8 columns
00	107	For no dark columns read, no row-wise noise correction applied

The vertical blanking and total frame time equations assume that the number of integration rows (bits 11 through 0 of Reg0x09) is less than the number of active plus blanking rows (Reg0x03 + 1 + Reg0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 5.

Table 5: Frame Time—Master Clock

Parameter	Name	Equation (master clock)	Default Timing
V'	Vertical Blanking (long integration time)	(Reg0x09 - Reg0x03) x (A + Q) + (Q - 2 x P)	25,868 pixel clocks = 51,736 master = 1.92 ms
F'	Total Frame Time (long integration time)	(Reg0x09 + 1) x (A + Q)	449,956 pixel clocks = 899,912 master = 33.33ms

Serial Bus Description

Registers are written to and read from the MT9V011 through the two-wire serial interface bus. The sensor is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out through the MT9V011 serial data (SDATA) line. The SDATA line is pulled up to VDD off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16 bits wide, and can be accessed through 16- or 8-bit two-wire serial bus sequences.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(n) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9V011 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit. The MT9V011 allows for 8-bit data transfers through the two-wire serial interface by writing (or reading) the most significant eight bits to the register and then writing (or reading) the least significant eight bits to Reg0x80 (128).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A “0” in the LSB of the address indicates write mode, and a “1” indicates read mode. The write address of the sensor is 0xBA, while the read address is 0xBB.

Data Bit Transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock—it can only change when the two-wire serial interface clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-Acknowledge Bit

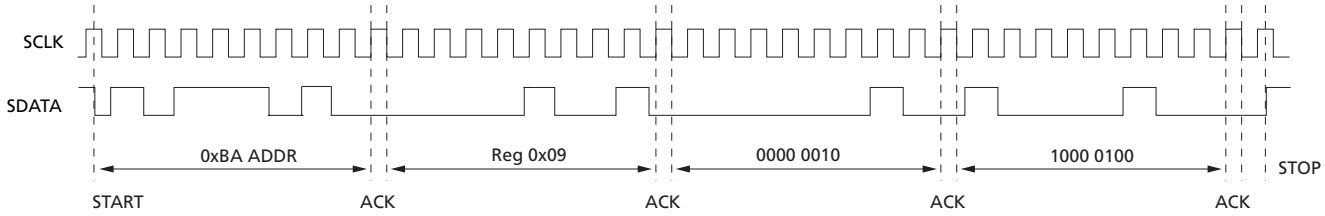
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Read and Write Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 9. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

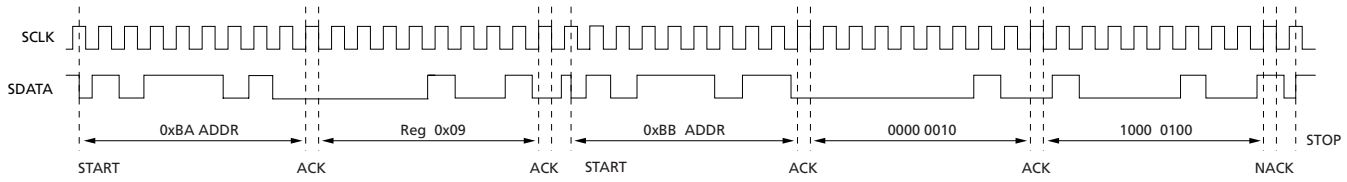
Figure 9: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 10. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

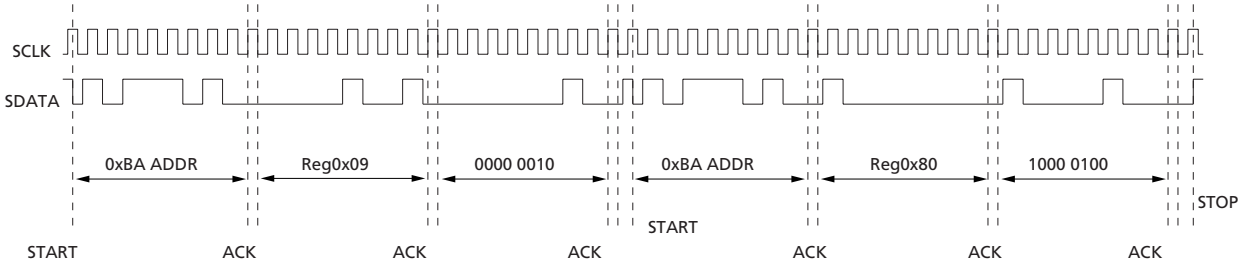
Figure 10: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284



Eight-Bit Write Sequence

To be able to write one byte at a time to the register a special register address is added. The 8-bit write is done by first writing the upper eight bits to the desired register and then writing the lower eight bits to the special register address (Reg0x80). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 11 a typical sequence for 8-bit writing is shown. The second byte is written to the special register (Reg 0x80).

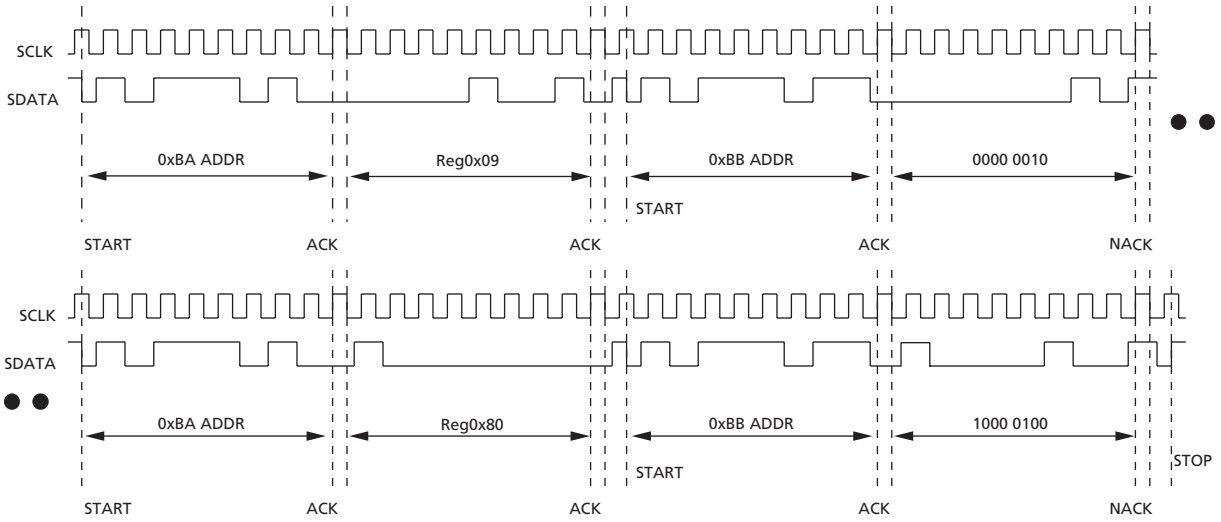
Figure 11: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



Eight-Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper eight bits are read from the desired register. By following this with a read from the special register (Reg0x80) the lower eight bits are accessed (Figure 12). The master sets the no-acknowledge bits shown.

Figure 12: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284



Feature Description

Window Control

Reg0x01 Row Start, Reg0x02 Column Start, Reg0x03 Window Height (row size), and Reg0x04 Window Width (column size)

These registers control the size and starting coordinates of the window. By changing these registers, any image format smaller than or equal to VGA can be specified.

Blanking Control

Reg0x05 Horizontal Blanking, and Reg0x06 Vertical Blanking

Blanking Control:

These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking).

- Horizontal blanking is specified in terms of pixel clocks.
- Vertical blanking is specified in terms of row readout times. (The programmed value is one less than the actual value.)

The actual imager timing can be calculated using Table 3 on page 12 which describes "Row Timing and FRAME_VALID/LINE_VALID Signals."

The number of dark rows read out depends on the vertical blanking set as shown in the Table 6.

Table 6: Vertical Blanking

Reg0x06	# dark rows
0	0
1-2	2
3+	4

Pixel Integration Control

Reg0x09 Shutter Width, and Reg0x0C Shutter Delay

These registers (along with the Window Size and horizontal blanking registers) control the integration time for the pixels.

Reg0x09: number of rows of integration, default = 0x01FC (508)
Reg0x0C: reset delay, default = 0x0000 (0). This is the number of master clocks that the timing and control logic waits before asserting the reset for a given row.

The actual total integration time, ^{t}INT, is:

^{t}INT =

Reg0x09 x Row Time - Overhead time - Reset delay, where:
Row Time = (Reg0x04 + 1 + 113 + Reg0x05) x (Reg0x0A + 2) master clock periods
Overhead time = K x 57 master clock periods
Reset delay = K x Reg0x0C master clock periods

If the value in Reg0x0C exceeds (row time - 444)/K master clock cycles, the row time will be extended by (K x Reg0x0C - (row time - 444)) clock cycles.

Where :

K = 4 when Reg0x07[4] = 0, and

K = 2 when Reg0x07[4] = 1

In this expression the row time term corresponds to the number of rows integrated. The overhead time is the time between the READ cycle and the RESET cycle, and the final term is the effect of the reset delay.

Typically, the value of Reg0x09 (Shutter Width) is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the MT9V011 will add additional blanking rows as needed. A second constraint is that ^{t}INT must be adjusted to avoid banding in the image from light flicker. Under 60 Hz flicker, this means ^{t}INT must be a multiple of 1/120 of a second. Under 50 Hz flicker, ^{t}INT must be a multiple of 1/100 of a second.

Pixel Clock Speed

Reg0x0A Pixel Clock Speed

The pixel clock speed is set by Reg0x0A. The pixel clock period will be the number set plus two master clock cycles. The default value is 0, which is equal to 2 master clock cycles. With a master clock frequency of 27 MHz the PIXCLK frequency will be 13.5 MHz. The pixel clock out can be shifted relative to the data out by setting bit 8-11 of Reg0x07 appropriately.

Reset

Reg0x0D Reset

This register is used to reset the sensor to its default, power-up state. To reset the MT9V011, first write a “1” into bit 0 of this register, then write a “0” into bit 0 to resume operation.

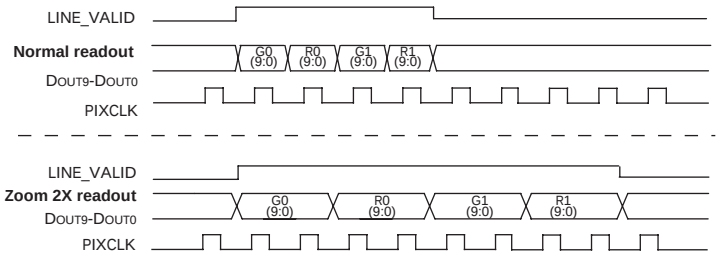
Digital Zoom

Reg0x1E Digital Zoom/True decimation

In zoom mode, the pixel data rate is slowed down by a factor of either 2 or 4, and either 1 or 3 additional blank rows are added between each output row. This is designed to give the controller logic time to repeat data to fill in a window that is either 2 or 4 times larger with repeated data.

The pixel clock speed is not affected by this operation, and the output data for each pixel is valid for either 2 or 4 pixel clocks. In zoom by 2 mode, every row is followed by a blank row (with its own line valid, but all data bits = 0) of equal time. In zoom by 4 mode, every row is followed by three blank rows. The combination of this register and an appropriate change to the window sizing registers allows the user to zoom to a region of interest without affecting the frame rate.

Figure 13: Readout of 4 Pixels in Normal and Zoom 2x Output Mode

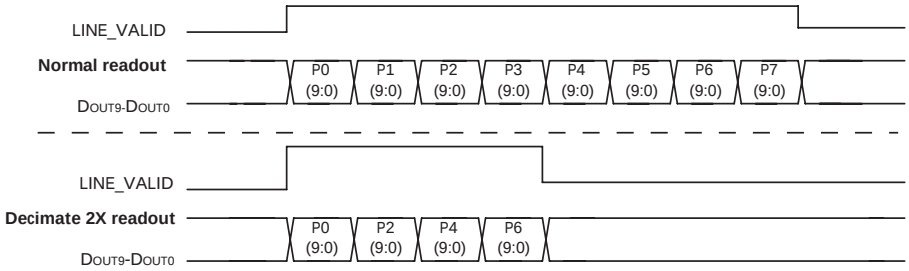


True Decimation mode

Reg0x1E Digital Zoom/True decimation

True decimation mode is intended for use in sensors without color filtering. There are three modes with different amount of decimation. In decimate 2x every other column and row are skipped. In decimate 4x three rows/columns will be skipped for every row/column read out, and in decimate 8x seven rows/columns will be skipped for every row/column read out. Decimate 2x is shown in Figure 14. In decimation mode the global gain register should be used to set the gain.

Figure 14: Readout of 8 Pixels in Normal and 2x Decimation Output Mode

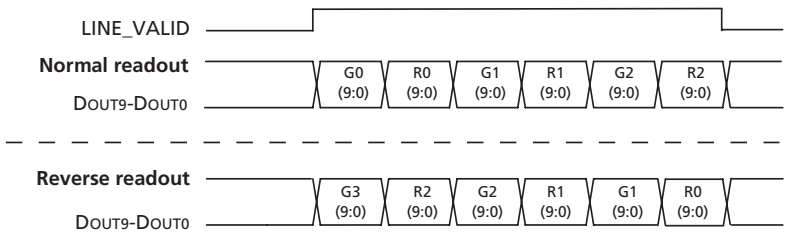


Read Mode

Column Mirror image

By setting bits 14 and 5 of Reg0x20 the readout order of the columns will be reversed, as shown in Figure 15.

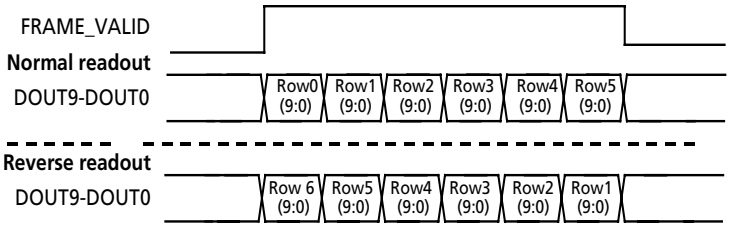
Figure 15: Readout of 6 Pixels in Normal and Column Mirror Output Mode



Row Mirror Image

By setting bits 15 and 7 of Reg0x20 the readout order of the rows will be reversed, as shown in Figure 16.

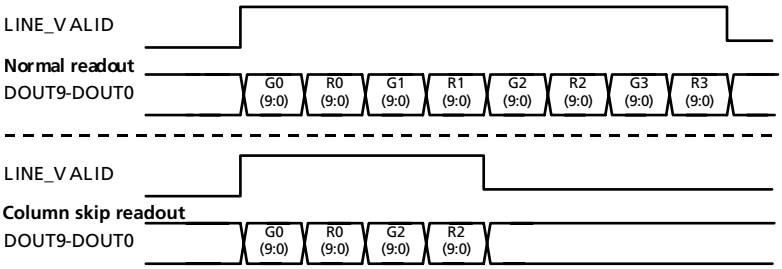
Figure 16: Readout of 6 Rows in Normal and Row Mirror Output Mode



Column and Row Skip

By setting bit 3 of Reg0x20 only half of the columns set will be read out, as shown in Figure 17. The row skip works in the same way and will only read out two out of four rows. For both row and column skip the number of rows/columns read out will be half of what is set in Reg0x03 and Reg0x04.

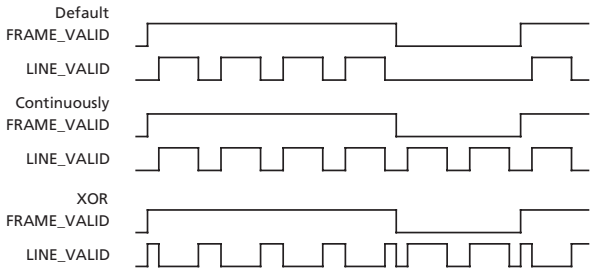
Figure 17: Readout of 8 Pixels in Normal and Column Skip Output Mode



Line Valid

By setting bit 9 and 10 of Reg0x20 the line valid signal can get three different output formats. The formats are shown in Figure 18 when reading out four rows and two vertical blanking rows. In the last format the line valid signal is the XOR between the continuously line valid signal and the frame valid signal.

Figure 18: Different Line Valid Formats



Recommdended Gain Settings

The gains for green1, blue, red, and green2 pixels are set by registers Reg0x2B, Reg0x2C, Reg0x2D, and Reg0x2D, respectively. Gain can also be set globally by Reg0x35. The analog gain is set by bits[8:0] of the corresponding register as following:

Gain = (Bit[8] + 1) x (Bit[7] + 1) x (Bit[6:0]/32)

Digital gain is set by bits 9 and 10 of the same registers.

The analog gain circuitry (pre-ADC) is designed to offer signal gains from 1 to 15.875.

The minimum gain of 1 (register set to 0x0020) corresponds to the lowest setting where the pixel signal is guaranteed to saturate the ADC under all specified operating conditions. Any reduction of the gain below this value may cause the sensor to saturate at ADC output values less than the maximum, under certain conditions. It is recommended that this guideline be followed at all times.

Since bits 7 and 8 of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, while the same overall gain. Table 7 lists the recommended gain settings.

Table 7: Recommended Gain Settings

Desired Gain	Recommended Settings (Gain Registers)	Conversion Formula (Arithmetic)
1.000 to 1.969	0x0020 to 0x003F	(Register value)/32
2.000 to 7.938	0x00A0 to 0x00FF	(Register value - 128)/16
8.000 to 15.875	0x01C0 to 0x01FF	(Register value - 384)/8

Electrical Specifications

Table 8: DC Electrical Characteristics
(V_{DD} = V_{AA} = 2.8 ±0.25V; T_A = Ambient = 25°C; 30 fps at 27 MHz)

Symbol	Definition	Condition	Min	Typ	Max	Unit	notes
V_{IH}	Input High Voltage		V_{DD}-0.25		V_{DD}+0.25	V	
V_{IL}	Input Low Voltage		-0.3		0.8	V	
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{DD} or V_{GND}	-5		5	µA	
V_{OH}	Output High Voltage		V_{DD}-0.2			V	
V_{OL}	Output Low Voltage				0.2	V	
I_{OH}	Output High Current				5.0	µA	
I_{OL}	Output Low Current				5.0	µA	
I_{OZ}	Tri-state Output Leakage Current				5.0	µA	
I_{AA}	Analog Operating Current	CLKIN = 27 MHz; default setting, C_{LOAD} = 10pF	14.0	20.0	28.0	mA	
I_{DD}	Digital Operating Current	CLKIN = 27 MHz; default setting, C_{LOAD} = 10pF	3.0	5.0	8.0	mA	
I_{AA} Standby	Analog Standby Supply Current	STDBY = V_{DD}	0.0	0.0	5.0	µA	1, 2
I_{DD} Standby	Digital Standby Supply Current	STDBY = V_{DD}	0.0	1.0	5.0	µA	1, 2

Notes:
1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.
2. When STANDBY is de-asserted, standby mode is exited immediately (within several master clocks), but the current frame and the next two frames will be invalid. The fourth frame will contain a valid image.

Table 9: AC Electrical Characteristics
(V_{DD} = V_{AA} = 2.8 ±0.25V; T_A = Ambient = 25°C)

Symbol	Definition	Condition	Min	Typ	Max	Unit	notes
f_{CLKIN}	Input Clock Frequency			27	27	MHz	
	Clock Duty Cycle		45	50	55	%	1
t_R	Input Clock Rise Time			2.5		ns	
t_F	Input Clock Fall Time			2.0		ns	
t_{PLHP} t_{PHLP}	CLKIN to PIXCLK propagation delay: LOW-to-HIGH HIGH-TO-LOW	C_{LOAD} = 10pF		 12.0 10.0		ns	
t_{DSETUP} t_{DHOLD}	PIXCLK to D_{OUT}(9:0) Setup Time Hold Time	C_{LOAD} = 10pF		 15.0 14.0		ns	
t_{OH}	Data Hold Time from CLKIN			9.0		ns	
$t_{PLHF,L}$ $t_{PHLF,L}$	CLKIN to FRAME_VALID and LINE_VALID propagation delay: LOW-to-HIGH, HIGH-to-LOW	C_{LOAD} = 10pF		 12.0 11.0		ns	
t_{PLHD} t_{PHLD}	CLKIN to D_{OUT} (9:0) propagation delay: LOW-to-HIGH, HIGH-to-LOW	C_{LOAD} = 10pF		 7.5 7.0		ns	
t_{OUTR}	Output Rise Time	C_{LOAD} = 10pF		7.0		ns	
t_{OUTF}	Output Fall Time	C_{LOAD} = 10pF		9.0		ns	

Notes: 1. For 30 fps operation with a 27 MHz clock, it is very important to have a precise duty cycle equal to 50%. With a slower frame rate and a slower clock the clock duty cycle can be relaxed.

Propagation Delays for PIXCLK and Data Out Signals

The typical output delay, relative to the master clock edge, is 7.5 ns. Note that the data outputs change on the falling edge of the master clock, with the pixel clock rising on the subsequent rising edge of the master clock.

Propagation Delays for FRAME_VALID and LINE_VALID Signals

The LINE_VALID and FRAME_VALID signals change on the same falling master clock edge as the data output. The LINE_VALID goes HIGH on the same falling master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock falling edge as the end of the output of the last valid pixel's data.

As shown in the “Output Data Timing” on page 11, FRAME_VALID goes HIGH 6 pixel clocks prior to the time that the first LINE_VALID goes HIGH. It returns LOW at a time corresponding to 6 pixel clocks after the last LINE_VALID goes LOW.

Figure 19: Propagation Delays for PIXCLK and Data Out Signals

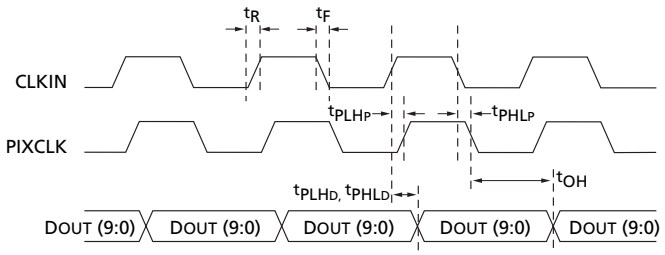


Figure 20: Propagation Delays for FRAME_VALID and LINE_VALID Signals

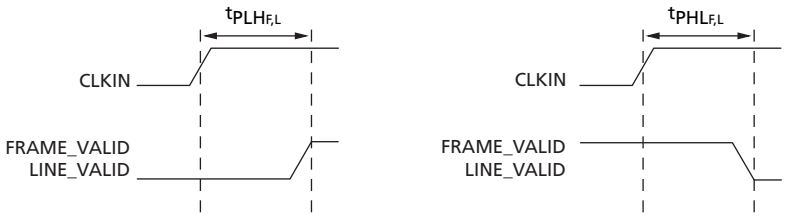
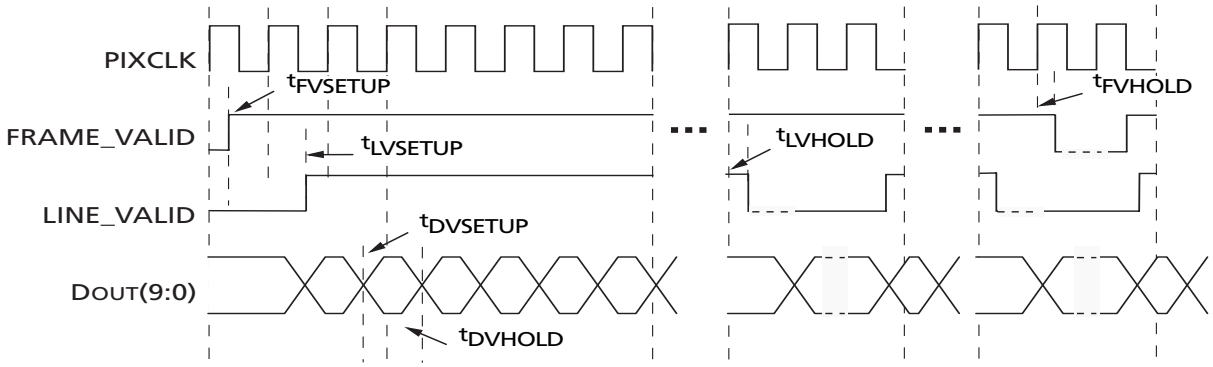


Figure 21: Data Output Timing Diagram



PIXCLK = max. 27 MHz

$t_{FVSETUP}$ = / setup time for FRAME_VALID before rising edge of PIXCLK / = 18ns

t_{FVHOLD} = / hold time for FRAME_VALID after falling edge of PIXCLK / = 18ns

$t_{LVSETUP}$ = / setup time for LINE_VALID before rising edge of PIXCLK / = 18ns

t_{LVHOLD} = / hold time for LINE_VALID after falling edge of PIXCLK / = 18ns

t_{DSETUP} = / setup time for DOUT before rising edge of PIXCLK / = 13ns

t_{DHOLD} = / hold time for DOUT after falling edge of PIXCLK / = 13ns

Frame start: FF00 00A0

Line start: FF00 0080

Line end: FF00 0090

Frame end: FF00 0010

Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 22: Serial Host Interface Start Condition Timing

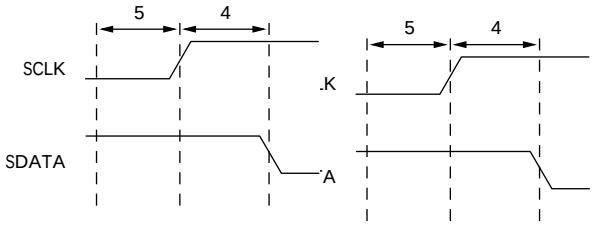
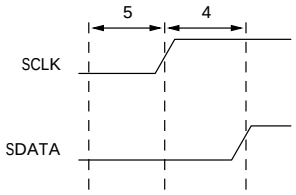
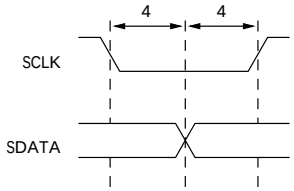


Figure 23: Serial Host Interface Stop Condition Timing



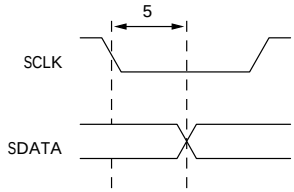
Note: All timing are in units of master clock cycle.

Figure 24: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 25: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 26: Acknowledge Signal Timing After an 8-bit Write to the Sensor

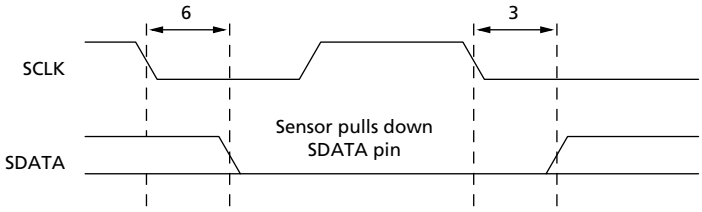
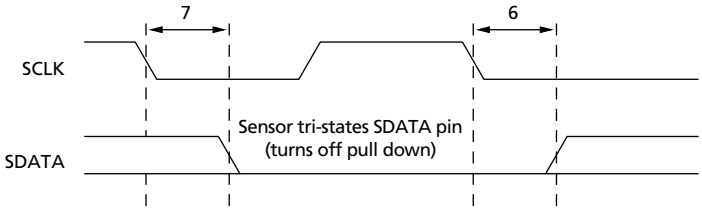


Figure 27: Acknowledge Signal Timing After an 8-bit Read from the Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float high. On the following cycle a start or stop bit may be used.

Figure 28: Spectral Response

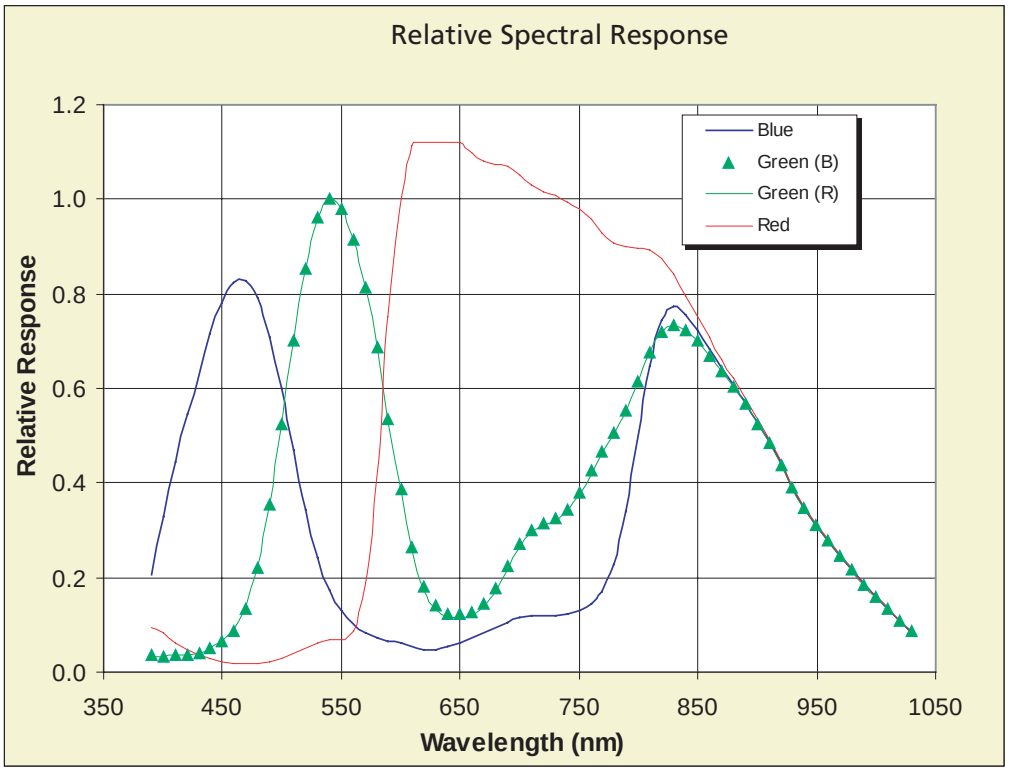
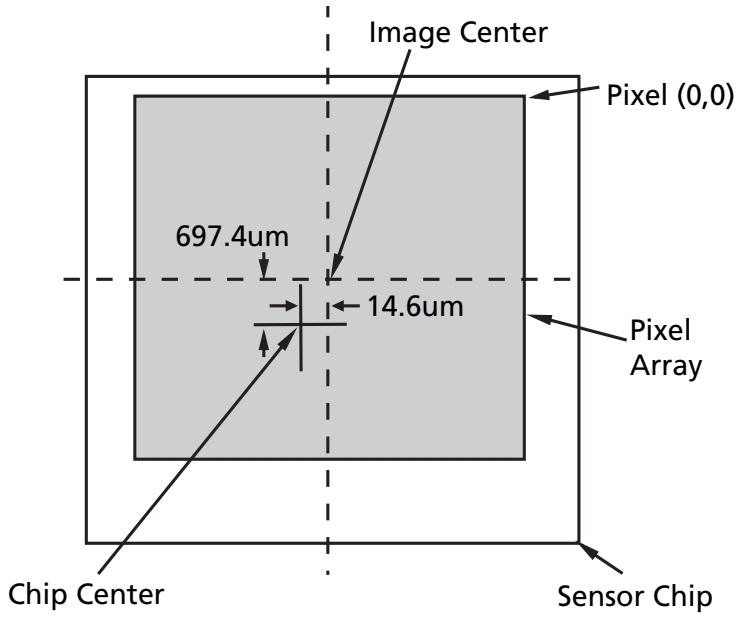
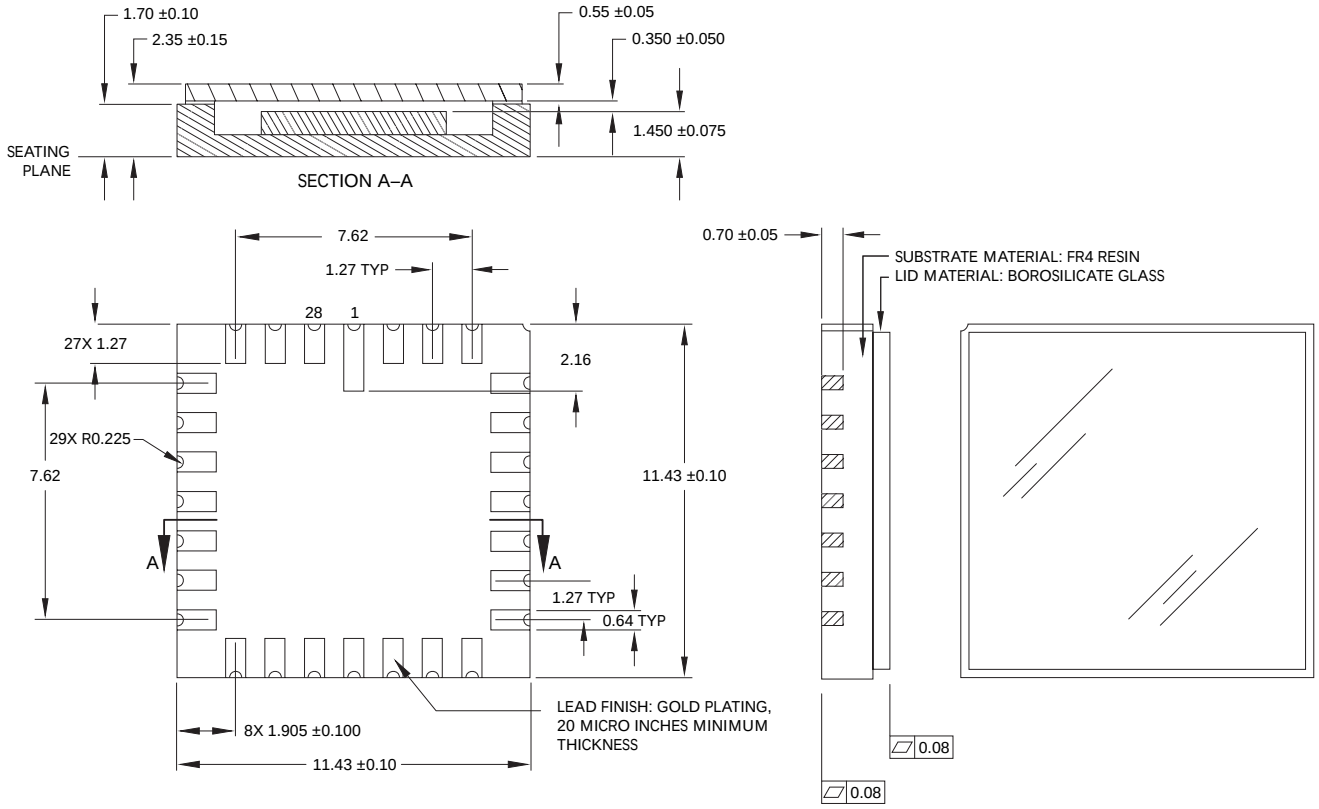


Figure 29: Image Center Offset



Note: Not to scale.

Figure 30: 28-Pin PLCC Package Outline Drawing



Note: All dimensions are in millimeters.

Revision History

Rev. D **5/12**

- Updated trademarks

Rev. C **6/10**

- Updated to non-confidential

Rev. B **5/10**

- Updated to Aptina template

Rev A, Preliminary **12/04**

- Initial Release of document

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