

SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163E – JULY 1993 – REVISED APRIL 2006

- Meets or Exceeds EIA Standard RS-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Support Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of -7 V to 12 V
- Positive- and Negative-Current Limiting
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)
- Functionally Interchangeable With SN75172

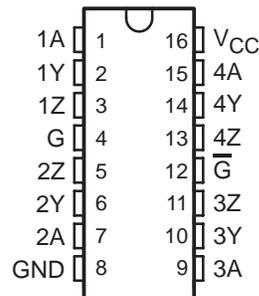
description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

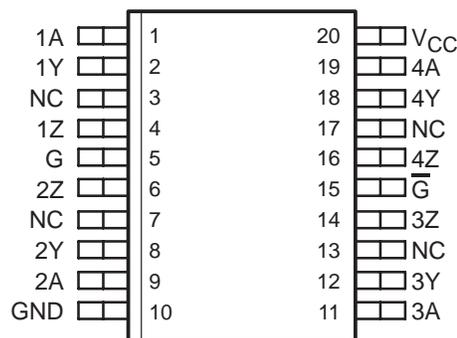
Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C . The SN65LBC172 is characterized over the industrial temperature range of -40°C to 85°C .

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUTS	
	G	\bar{G}	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



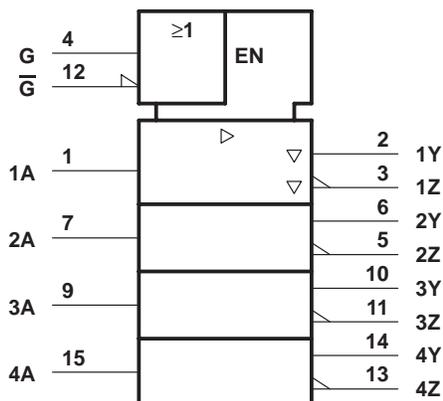
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SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

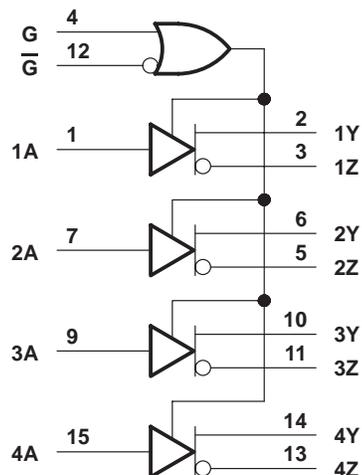
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logic symbol†

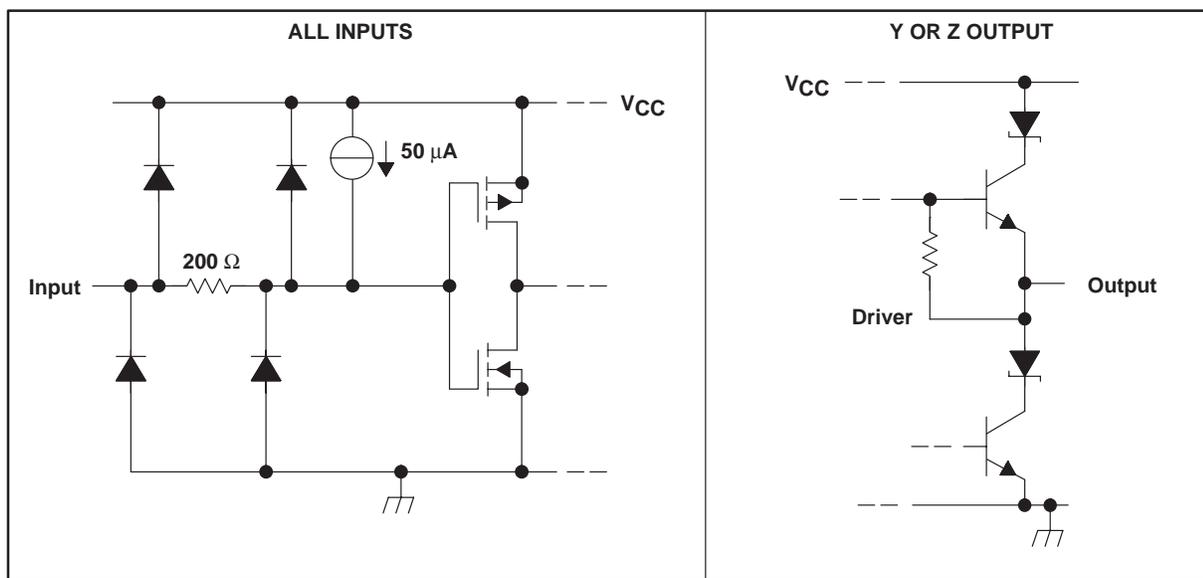


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



SN65LBC172, SN75LBC172

QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

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absolute maximum ratings†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Output voltage range, V_O	–10 V to 15 V
Voltage range at A, \bar{G} , G	–0.3 V to $V_{CC} + 0.5$ V
Continuous power dissipation	Internally limited‡
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}		0.8			V
Voltage at any bus terminal (separately or common mode), V_O	Y or Z	12			V
		–7			
High-level output current, I_{OH}	Y or Z	–60			mA
Low-level output current, I_{OL}	Y or Z	60			mA
Continuous total power dissipation		See Dissipation Rating Table			
Junction temperature, T_J		140			°C
Operating free-air temperature, T_A	SN65LBC172	–40			85
	SN75LBC172	0			70

DISSIPATION RATING TABLE

PACKAGE	THERMAL MODEL	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DW	Low K^\dagger	1094 mW	10.4 mW/°C	625 mW	469 mW
	High K^\ddagger	1669 mW	15.9 mW/°C	954 mW	715 mW
N		1150 mW	9.2 mW/°C	736 mW	598 mW

† In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51–3.

‡ In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51–7.



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA				-1.5	V
V _{OD}	Differential output voltage‡	R _L = 54 Ω, See Figure 1	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		R _L = 60 Ω, See Figure 2	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
Δ V _{OD}	Change in magnitude of common-mode output voltage§					±0.2	V
V _{OC}	Common-mode output voltage	R _L = 54 Ω,	See Figure 1			3 -1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage§					±0.2	V
I _O	Output current with power off	V _{CC} = 0, V _O = -7 V to 12 V				±100	μA
I _{OZ}	High-impedance-state output current	V _O = -7 V to 12 V				±100	μA
I _{IH}	High-level input current	V _I = 2.4 V				-100	μA
I _{IL}	Low-level input current	V _I = 0.4 V				-100	μA
I _{OS}	Short-circuit output current	V _O = -7 V to 12 V				±250	mA
I _{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal-transmission distance.

§ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{d(OD)}	Differential output delay time	R _L = 54 Ω,	See Figure 3	2	11	20	ns
t _{t(OD)}	Differential output transition time			10	15	25	
t _{pZH}	Output enable time to high level	R _L = 110 Ω,	See Figure 4		20	30	ns
t _{pZL}	Output enable time to low level	R _L = 110 Ω,	See Figure 5		21	30	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω,	See Figure 4		48	70	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω,	See Figure 5		21	30	ns



PARAMETER MEASUREMENT INFORMATION

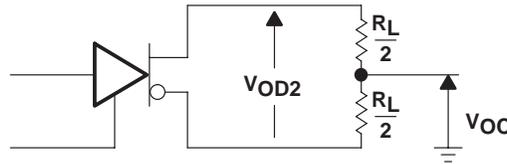
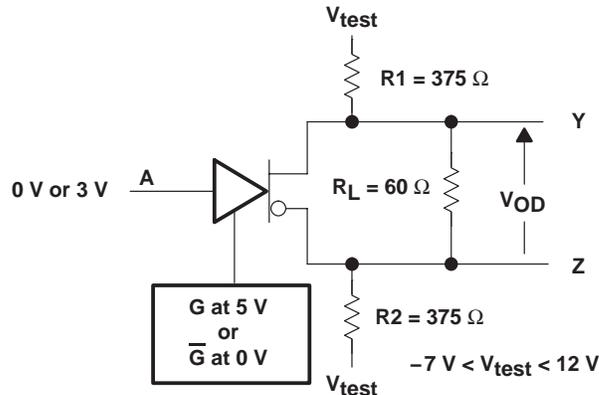
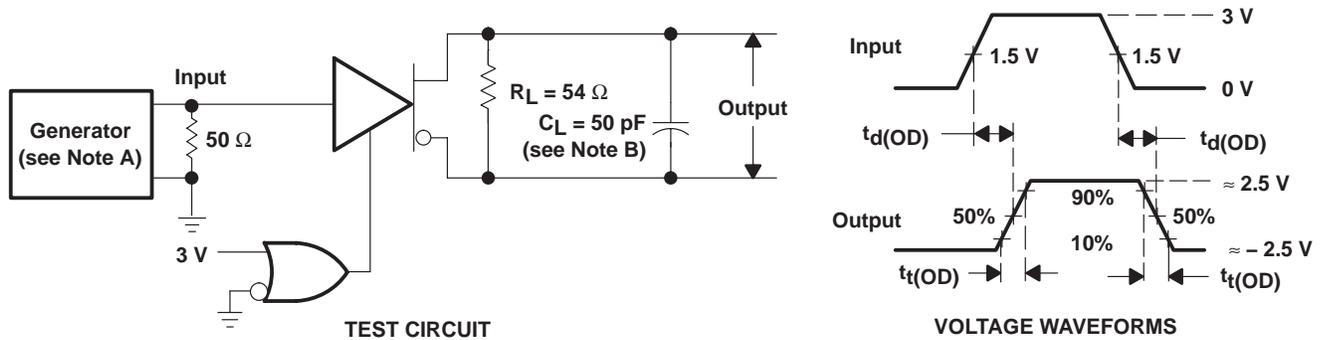


Figure 1. Differential and Common-Mode Output Voltages



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle = 50%, $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

Figure 2. Driver V_{OD} Test Circuit



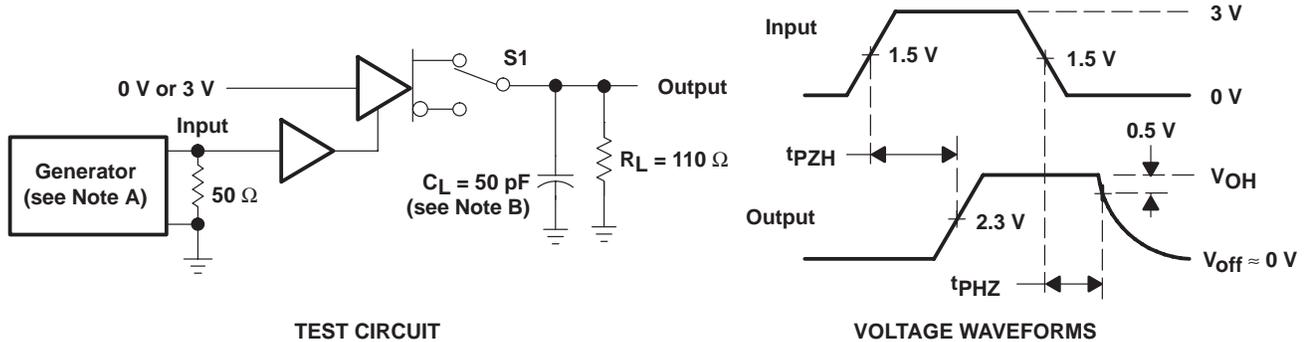
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle = 50%, $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

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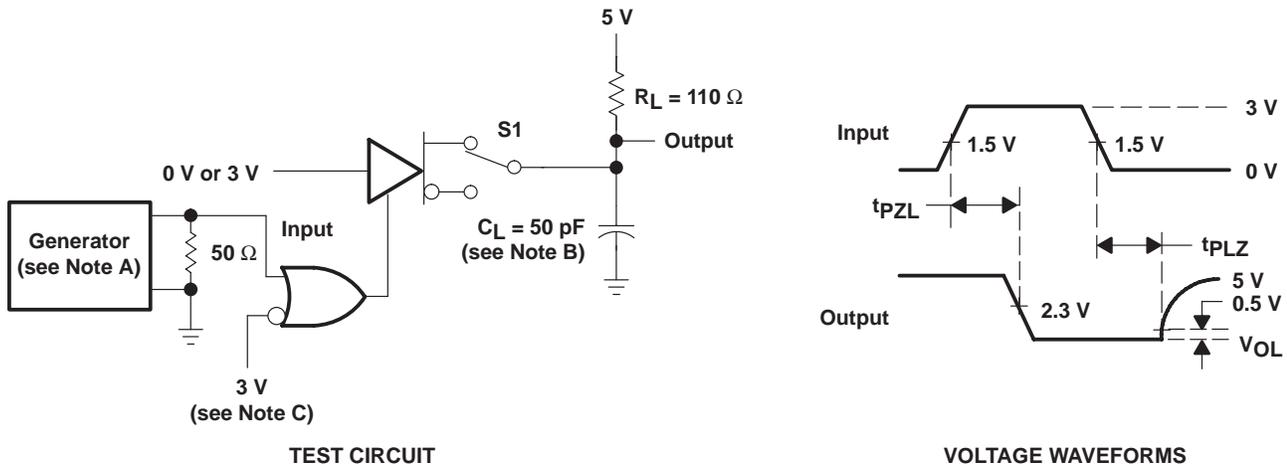
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_O = 50$ Ω .
- B. C_L includes probe and stray capacitance.

Figure 4. t_{pZH} and t_{pHZ} Test Circuit and Voltage Waveforms



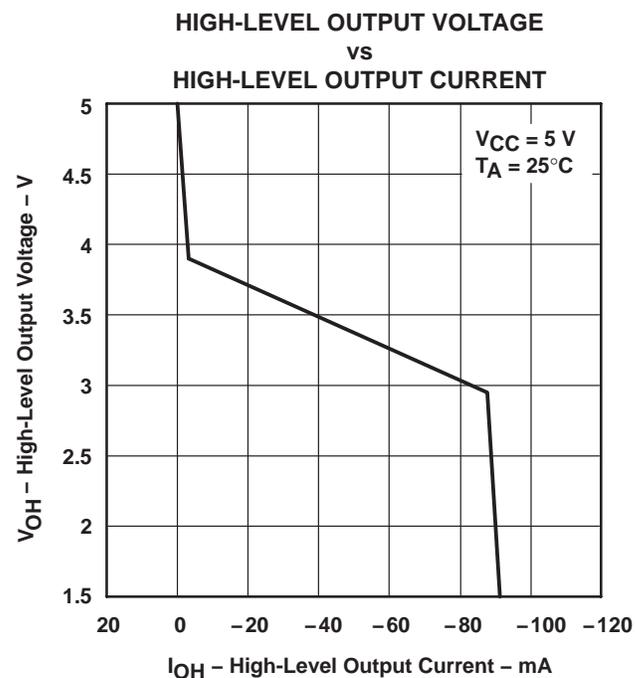
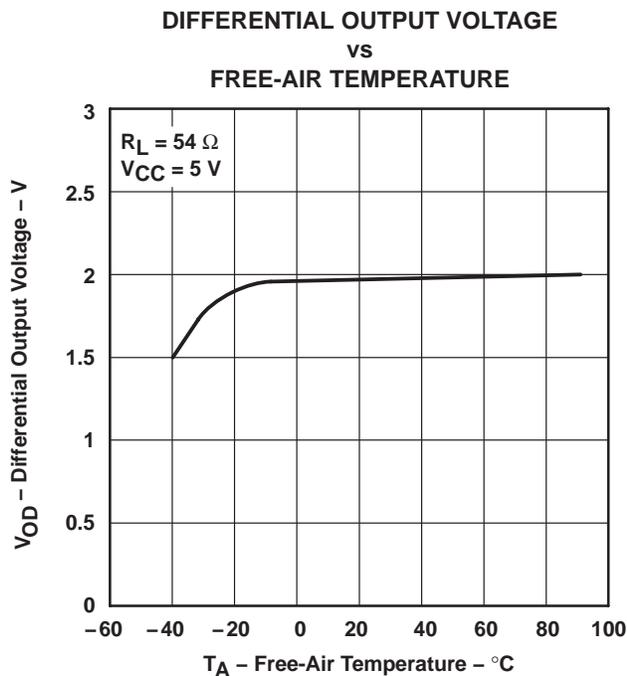
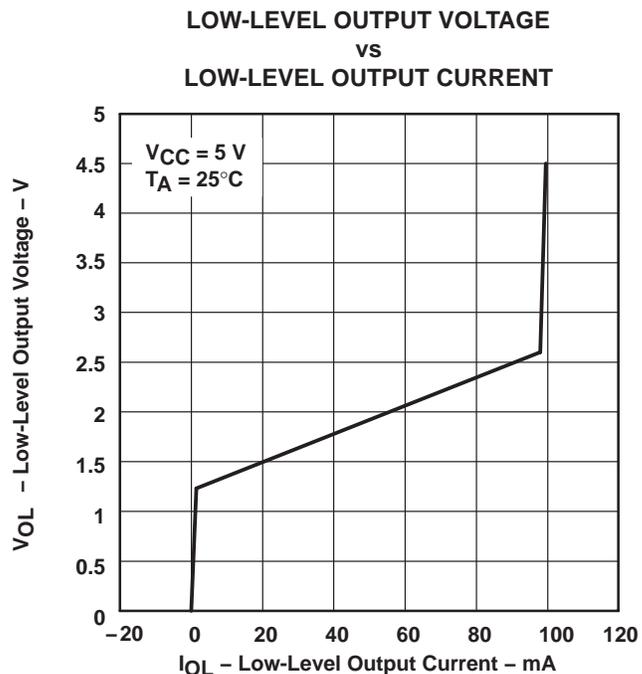
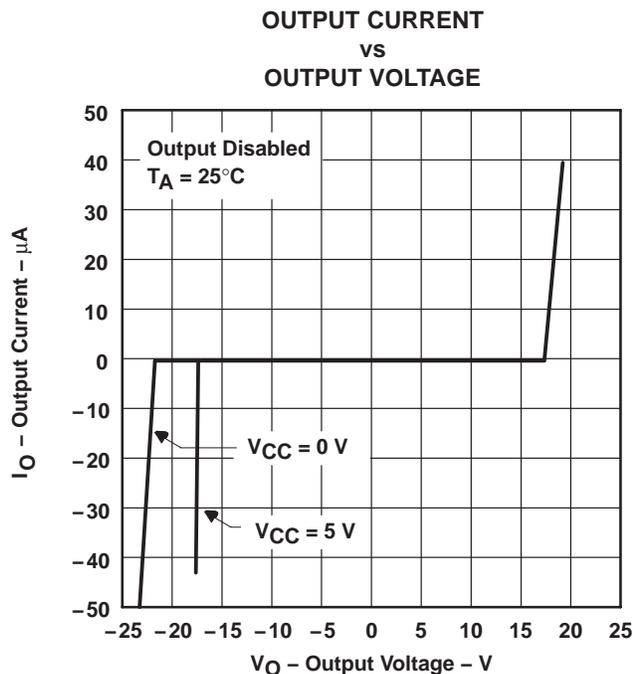
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_O = 50$ Ω .
- B. C_L includes probe and stray capacitance.
- C. To test the active-low enable \overline{G} , ground G and apply an inverted waveform to \overline{G} .

Figure 5. t_{pZL} and t_{pLZ} Test Circuit and Waveforms

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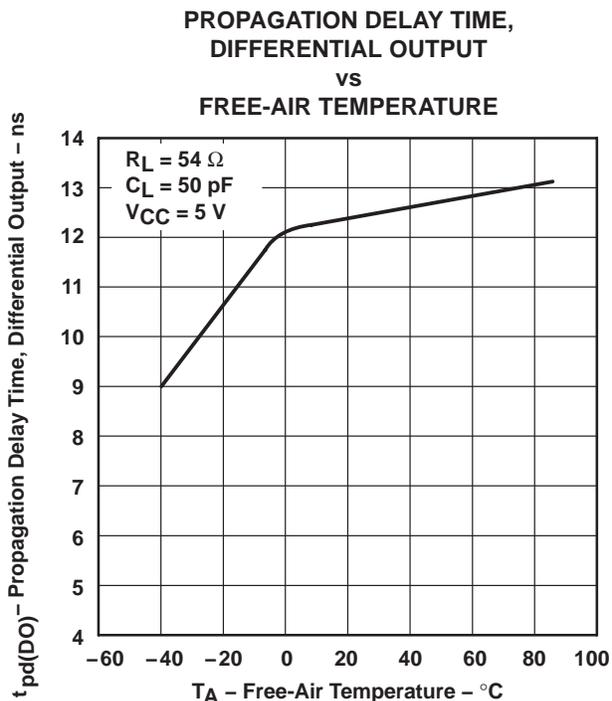
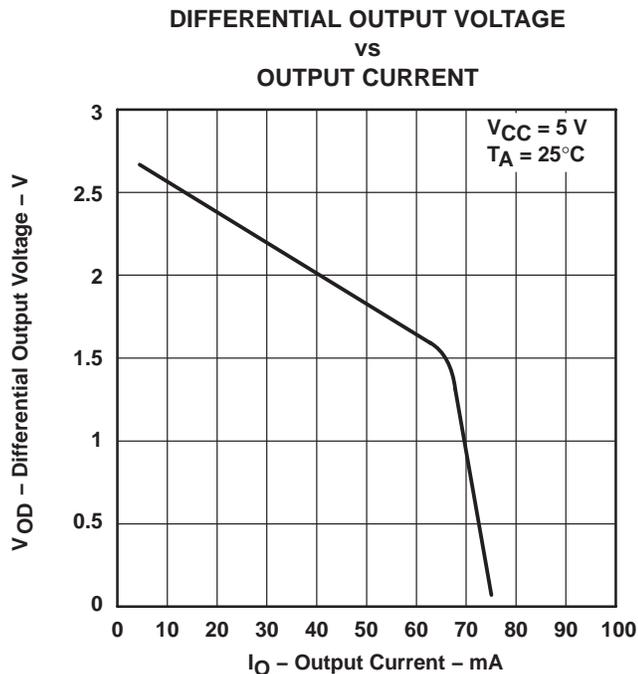
TYPICAL CHARACTERISTICS



SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

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TYPICAL CHARACTERISTICS



THERMAL CHARACTERISTICS – DW PACKAGE

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Junction-to-ambient thermal resistance, θ_{JA} †	Low-K board, no air flow		96		°C/W
	High-K board, no air flow		62.9		
Junction-to-board thermal resistance, θ_{JB}	High-K board, no air flow		39.6		°C/W
Junction-to-case thermal resistance, θ_{JC}			29.1		
Average power dissipation, $P_{(AVG)}$	All four channels maximum loading, maximum signaling rate, $R_L = 54 \Omega$, input to D is 10 Mbps 50% duty cycle square wave, $V_{CC} = 5.25 V$, $T_J = 130^\circ C$.			1100	mW
Ambient free-air temperature, T_A	JEDEC high-K board model	-40		85	°C
	JEDEC high-K board model	-40		64	
Thermal shutdown junction temperature, T_{SD}			165		°C

† See TI application note literature number SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.

THERMAL CHARACTERISTICS OF IC PACKAGES

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. Θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in Θ_{JA} can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 12).

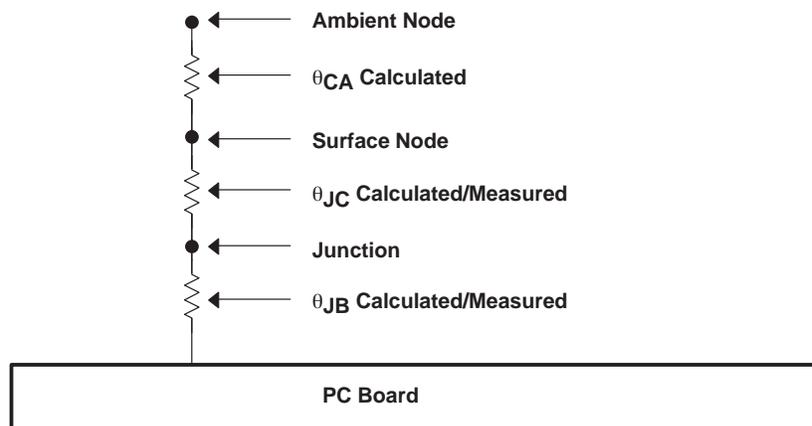


Figure 12. Thermal Resistance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC172DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC172	Samples
SN65LBC172N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC172N	Samples
SN75LBC172DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC172	Samples
SN75LBC172DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC172	Samples
SN75LBC172N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC172N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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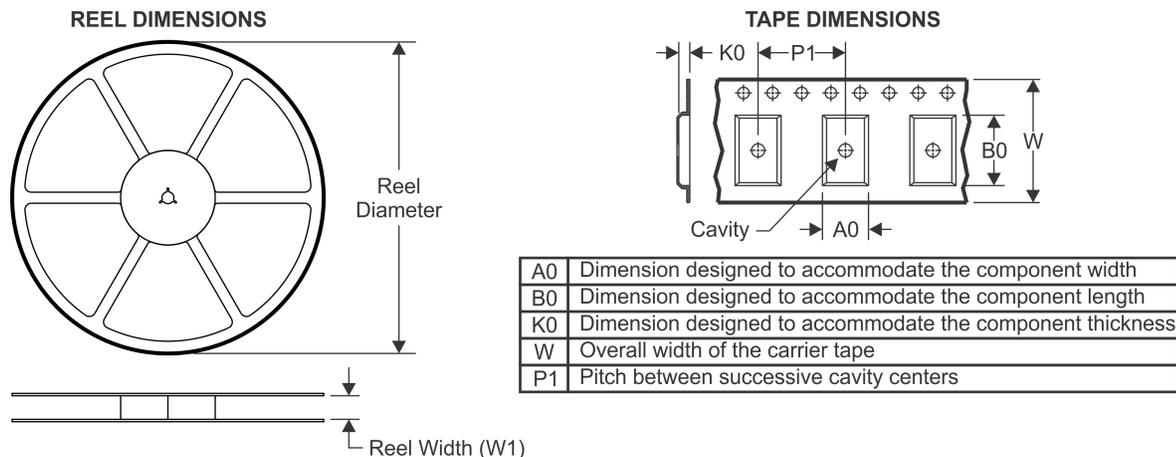
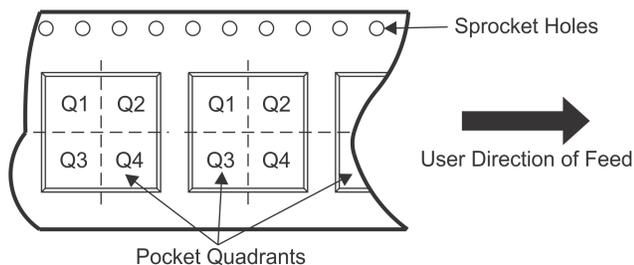
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN75LBC172 :

- Military: [SN55LBC172](#)

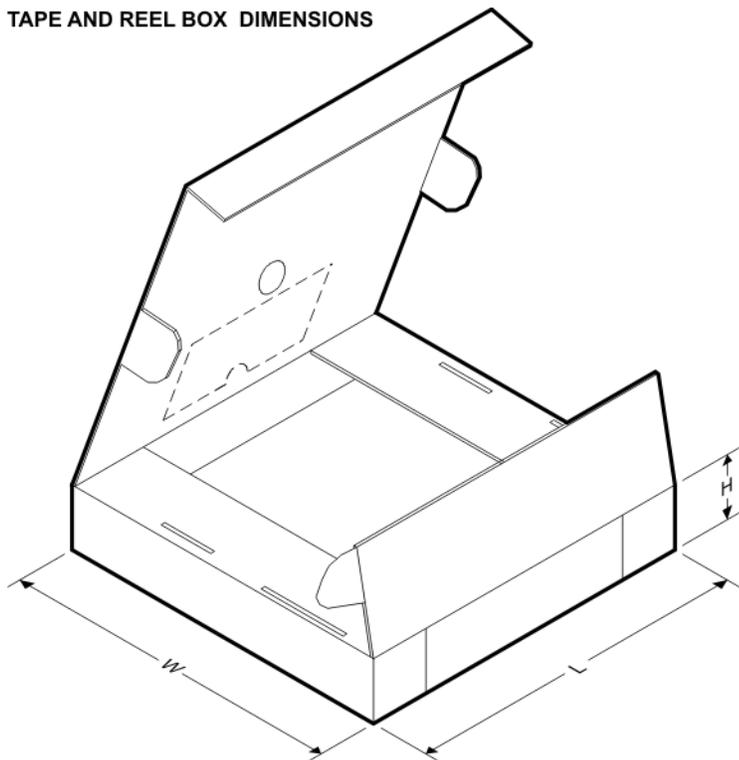
NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


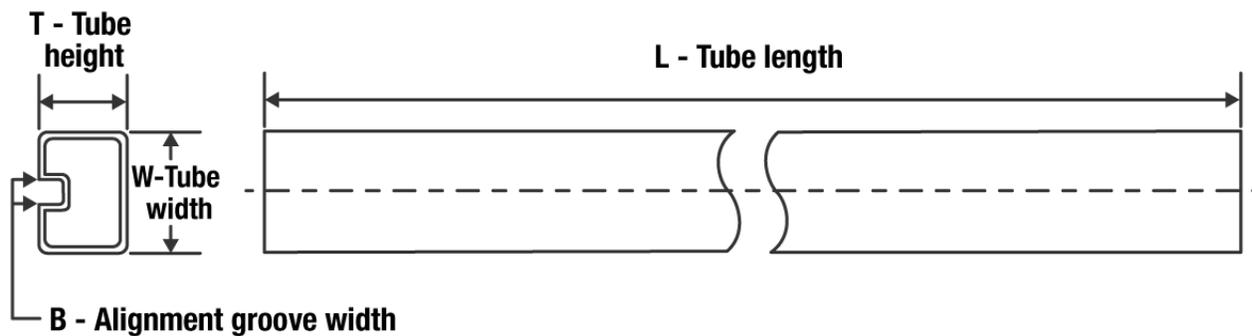
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC172DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE


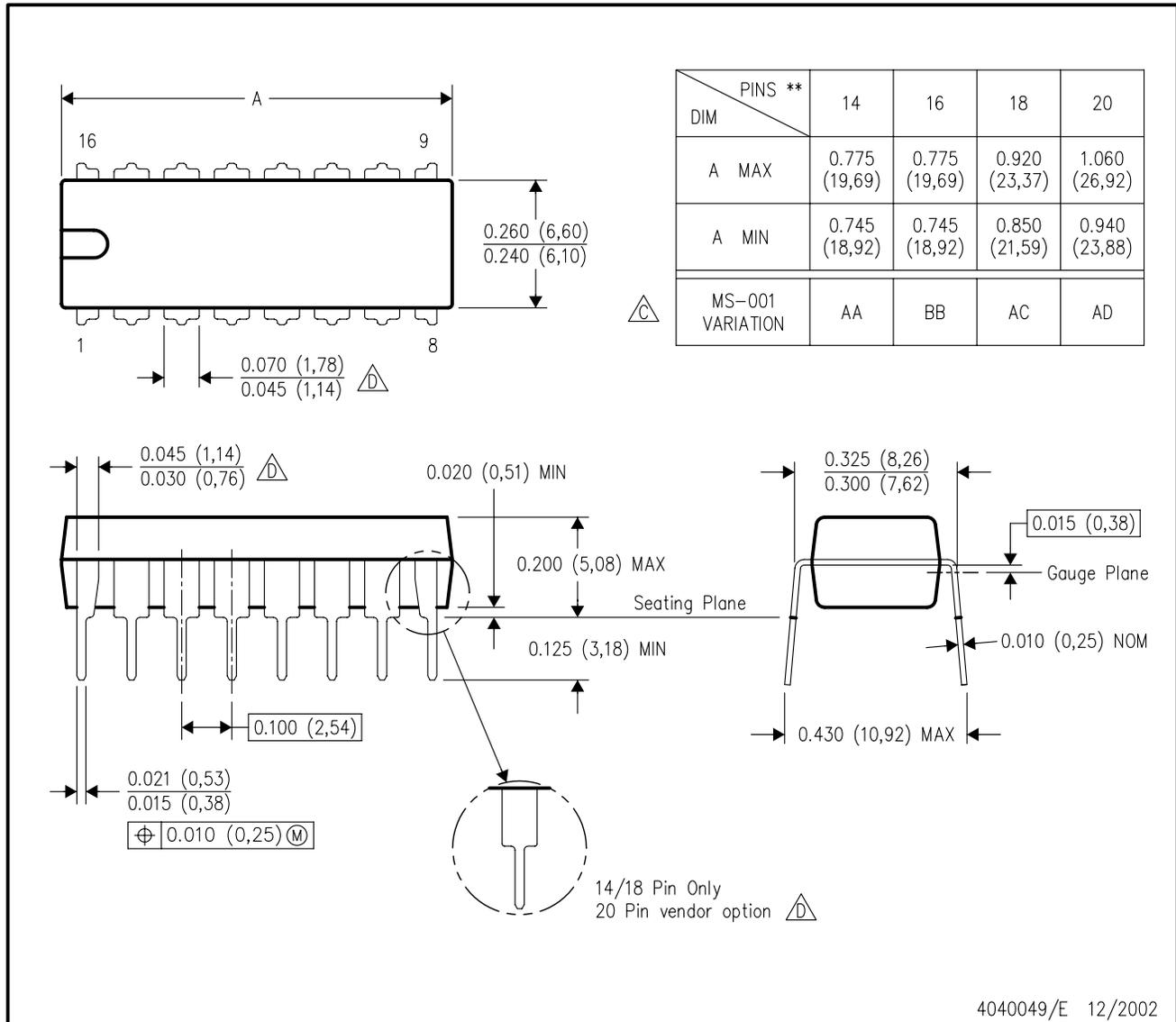
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC172DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN65LBC172DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN65LBC172N	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC172DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC172DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75LBC172N	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

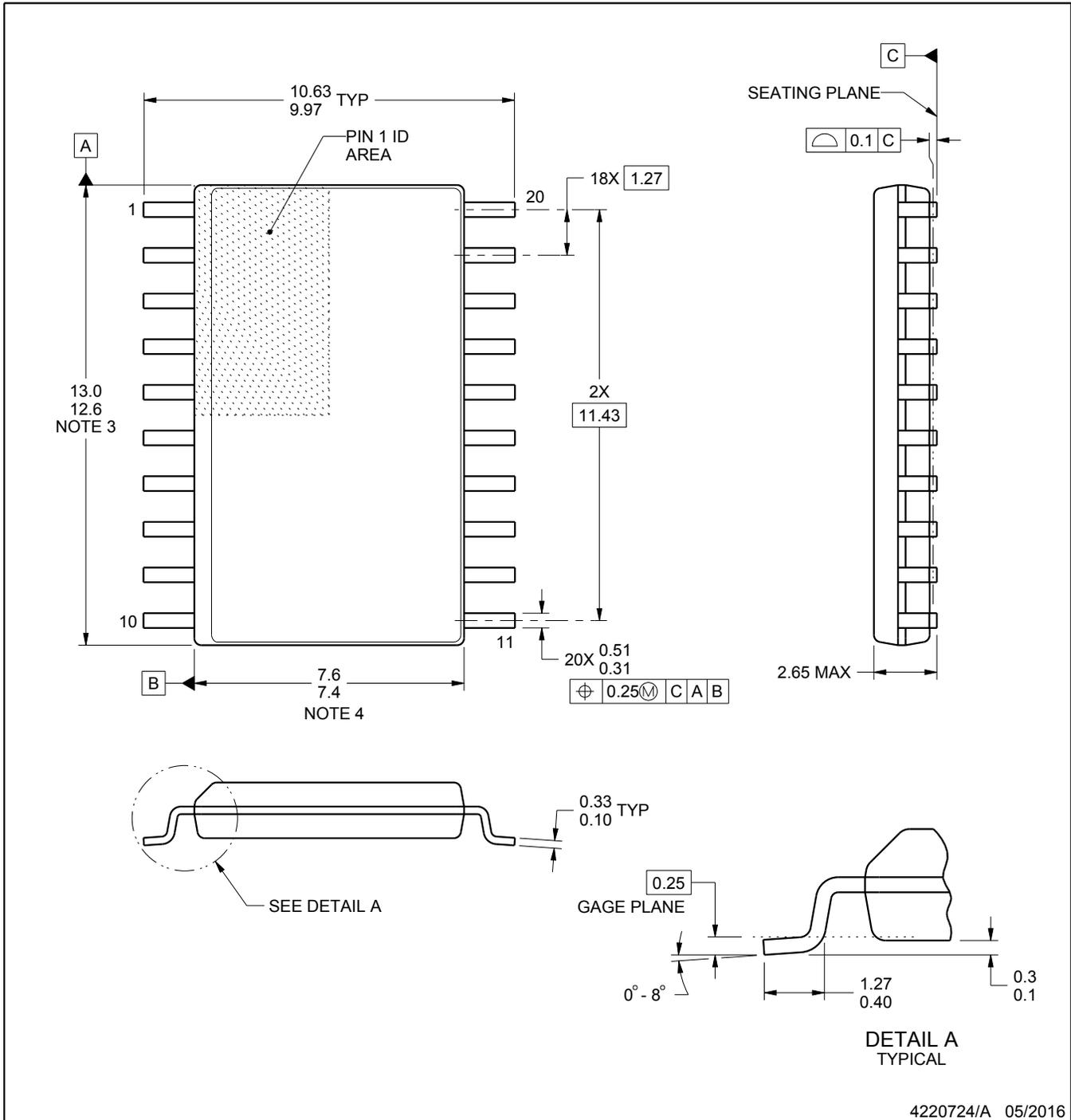
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

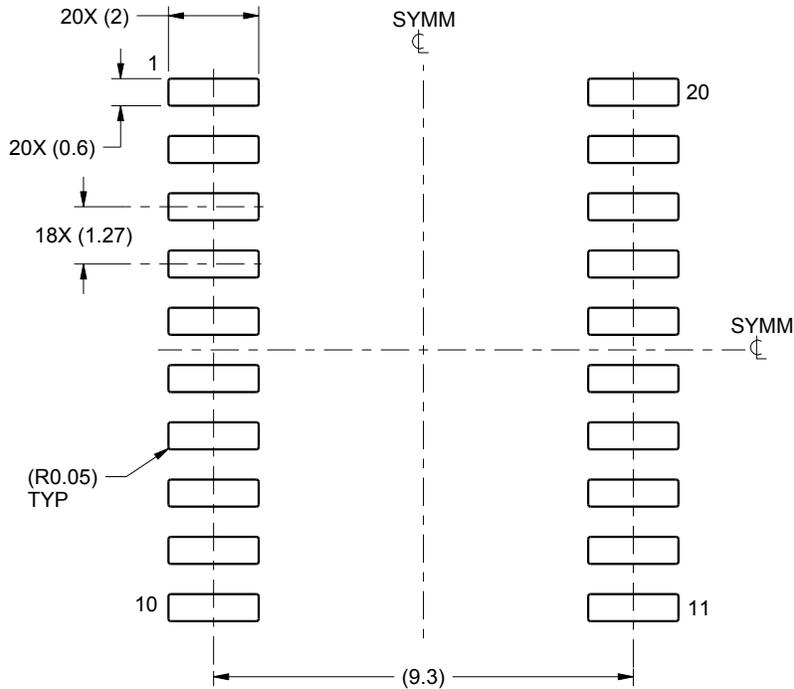
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

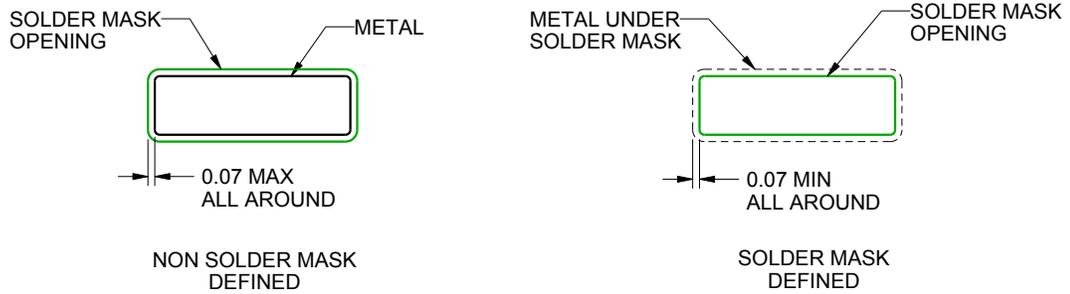
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

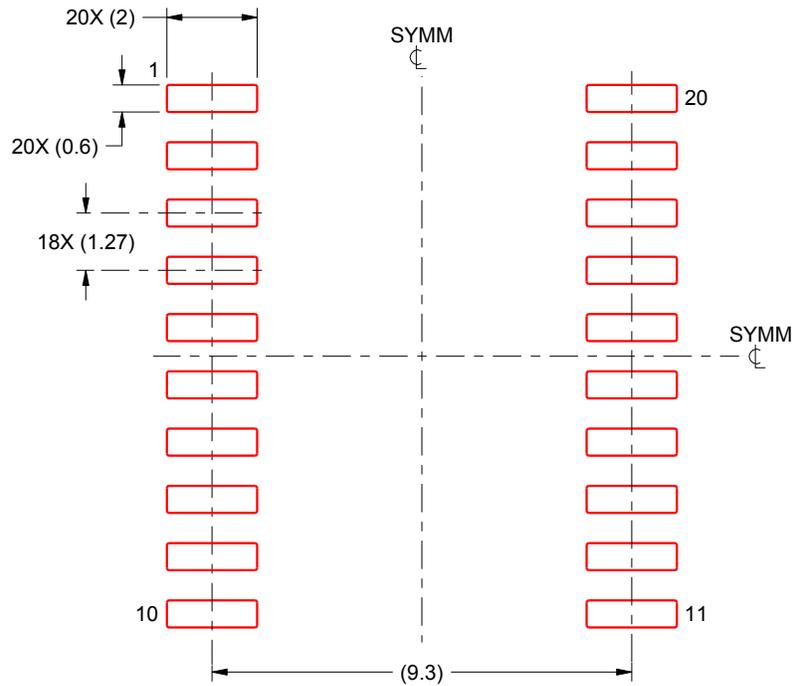
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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