3-Channel Constant Current LED Driver with Integrated Boost Controller

Check for Samples: LM3431

FEATURES

- **LM3431Q/LM3431AQ are Automotive Grade Products that are AEC-Q100 Grade 1 Qualified (–40°C to 125°C operating junction temperature)**
- **3-Channel Programmable LED Current**
- **High Accuracy Linear Current Regulation**
- **Analog and Digital PWM Dimming Control**
- **Up to 25kHz Dimming Frequency**
- **>100:1 Contrast Ratio**
- **Integrated Boost Controller**
- **5V-36V Input Voltage Range**
- **Adjustable Switching Frequency up to 1MHz**
- **LED Short and Open Protection**
- **Selectable Fault Shutdown or Automatic Restart**
- **Programmable Fault Delay**
- **Programmable Cycle by Cycle Current Limit**
- **Output Over Voltage Protection**
- **No Audible Noise**
- **Enable Pin**
- **LED Over-Temperature Shutdown Input**
- **Thermal Shutdown**
- **TSSOP-28 Exposed Pad Package**

DESCRIPTION

The LM3431 is a 3-channel linear current controller combined with a boost switching controller ideal for driving LED backlight panels in space critical applications. The LM3431 drives 3 external NPN transistors or MOSFETs to deliver high accuracy constant current to 3 LED strings. Output current is adjustable to drive strings in excess of 200 mA. The LM3431 can be expanded to drive as many as 6 LED strings.

The boost controller drives an external NFET switch for step-up regulation from input voltages between 5V and 36V. The LM3431 features LED cathode feedback to minimize regulator headroom and optimize efficiency.

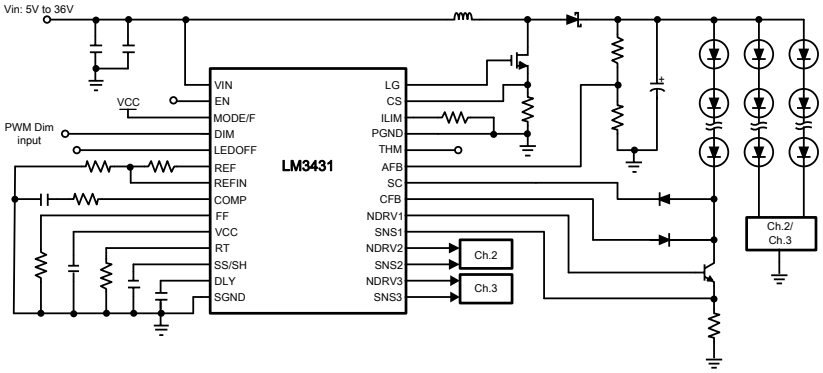
A DIM input pin controls LED brightness from analog or digital control signals. Dimming frequencies up to 25 kHz are possible with a contrast ratio of 100:1. Contrast ratios greater than 1000:1 are possible at lower dimming frequencies.

The LM3431 eliminates audible noise problems by maintaining constant output voltage regulation during LED dimming. Additional features include LED short and open protection, fault delay/error flag, cycle by cycle current limit, and thermal shutdown for both the IC and LED array. The enhanced LM3431A features reduced offset voltage for higher accuracy LED current.

APPLICATIONS

- **Automotive Infotainment Displays**
- **Small to Medium Format Displays**

TYPICAL APPLICATION CIRCUIT



CONNECTION DIAGRAM

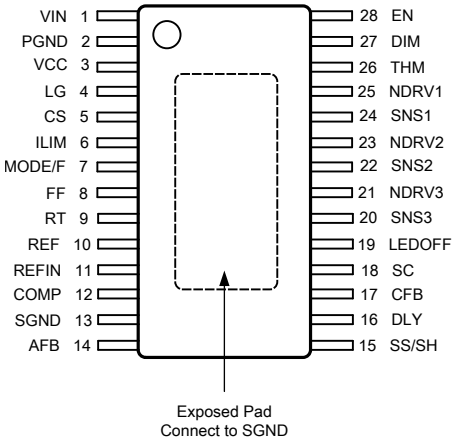


Figure 1. 28 Lead Plastic Exposed Pad TSSOP
Top View
See Package Number PWP0028A

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VIN	Power supply input.
2	PGND	Power ground pin. Connect to ground.
3	VCC	Internal reference voltage output. Bypass to PGND with a minimum 4.7 µF capacitor.
4	LG	Boost controller gate drive output. Connect to the NFET gate.
5	CS	Boost controller current sense pin. Connect to the top side of the boost current sense resistor.
6	ILIM	Boost controller current limit adjust pin. Connect a resistor from this pin to the Boost current sense resistor to set the current limit threshold.
7	MODE/F	Dimming mode selection pin. Pull high for digital PWM control. Or connect to a capacitor to GND to set the internal dimming frequency.
8	FF	Feedforward pin. Connect to a resistor to ground to control the output voltage over/undershoot during PWM dimming.
9	RT	Frequency adjust pin. Connect a resistor from this pin to ground to set the operating frequency of the boost controller.
10	REF	Reference voltage. Use this pin to provide the REFIN voltage.
11	REFIN	This pin sets the LED current feedback voltage. Connect to a resistor divider from the REF pin.
12	COMP	Output of the error amplifier. Connect to the compensation network.
13	SGND	Signal ground pin. Connect to ground.
14	AFB	Anode feedback pin. The boost controller voltage feedback during LED off time. Connect this pin to a resistor divider from the output voltage.
15	SS/SH	Soft-start and sample-hold pin. Connect a capacitor from this pin to ground to set the soft-start time.
16	DLY	Fault delay pin. Connect a capacitor from this pin to ground to set the delay time for shutdown.
17	CFB	Cathode feedback pin. The boost controller voltage feedback. Connect through a diode to the bottom cathode of each LED string.
18	SC	LED short circuit detection pin. Connect through a diode to the bottom cathode of each string.
19	LEDOFF	A dual function pin. The LEDOFF signal controls external drivers during PWM dimming. Or connect to ground to enable automatic fault restart.
20	SNS3	Current feedback for channel 3. Connect to the top of the channel 3 current sense resistor.
21	NDRV3	Base drive for the channel 3 current regulator. Connect to the NPN base or NFET gate.
22	SNS2	Current feedback for channel 2.
23	NDRV2	Base drive for the channel 2 current regulator.

PIN DESCRIPTIONS (continued)

Pin No.	Pin Name	Description
24	SNS1	Current feedback for channel 1.
25	NDRV1	Base drive for the channel 1 current regulator.
26	THM	LED thermal monitor input pin. When pulled below 1.2V, device enters standby mode.
27	DIM	PWM dimming input pin. Accepts a digital PWM or analog voltage level input to control LED current duty cycle.
28	EN	Enable pin. Connect to VIN through a resistor divider to set an external UVLO threshold. Pull low to shutdown.
EP		Exposed pad. Connect to SGND.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

If Military/Aerospace specified devices are required, contact the Texas Instruments Semiconductor Sales Office/ Distributors for availability and specifications.

		VALUE / UNIT
Voltages from the indicated pins to SGND:	VIN	–0.3V to 37V
	EN	–0.3V to 10V
	DIM	–0.3V to 7V
	MODE/F	–0.3V to 7V
	REFIN	–0.3V to 7V
	THM	–0.3V to 7V
	DLY	–0.3V to 7V
	SNSx	–0.3V to 7V
	NDRVx	–0.3V to 7V
	CFB	–0.3V to 7V
	SC	-0.3V to 40V
	AFB	–0.3V to 7V
	CS	–0.3V to 7V
	VCC	–0.3V to 7V
Storage Temperature		–65°C to +150°C
Soldering Dwell Time, Temperature	Infrared	20sec, 240°C
	Vapor Phase	75sec, 219°C
ESD Rating Human Body Model (2)		2 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the ELECTRICAL CHARACTERISTICS.
(2) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS (1)

	VALUE / UNIT
VIN	4.5V to 36V
Junction Temperature Range	-40°C to +125°C
Thermal Resistance (θ_{JA}) (2), TSSOP-28 (0.5W)	32°C/W
Power Dissipation (3), TSSOP-28	3.1W

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the ELECTRICAL CHARACTERISTICS.
(2) The Thermal Resistance specifications are based on a JEDEC standard 4-layer pcb. θ_{JA} will vary with board size and copper area.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\_MAX} = (T_{J\_MAX} – T_A)/\theta_{JA}$. The maximum power dissipation is determined using T_A = 25°C, and T_{J_MAX} = 125°C.

ELECTRICAL CHARACTERISTICS

Specifications in standard type are for T_J = 25°C only, and limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Unless otherwise stated, V_{IN} = 12V. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
SYSTEM						
I_Q	Operating VIN Current (2)	DIM = 5V		4.0	**4.85**	mA
I_{Q_SB}	Standby mode VIN current	EN = 1V		3.7		mA
I_{Q_SD}	Shutdown mode VIN Current	EN = 0V, Vin = 36V		15	**23**	µA
V_{CC}	VCC voltage	Iload = 25 mA, Vin = 5.5 to 36V	**4.80**	5	**5.24**	V
VCC_{ILIM}	VCC current limit			72		mA
UVLO	UVLO threshold	VIN rising, measured at VCC		4.36	**4.50**	V
	hysteresis			0.28		V
V_{EN_ST}	Enable pin Standby threshold	EN rising		0.75		V
V_{EN}	Enable pin On threshold	EN rising	**1.185**	1.230	**1.275**	V
	hysteresis			115	**165**	mV
LINEAR CURRENT CONTROLLER						
V_{REF}	Reference Voltage	IREF < 300 µA	**2.45**	2.5	**2.55**	V
I_{REFIN}	REFIN input bias current	REFIN = 300 mV		14	**80**	nA
$\Delta V_{REF} / \Delta V_{IN}$	Line regulation	5.5V < VIN < 36V		0.0001		%/V
V_{NDRV}	NDRVx drive voltage capability	INDRVx = 5 mA		3.7		V
I_{NDRV_SK}	NDRVx drive sink current	$NDRV_X$ = 0.9V	**4**	6	**8**	mA
I_{NDRV_SC}	NDRVx drive source current	$NDRV_X$ = 0.9V	**10**	15	**20**	mA
I_{SNS}	SNSx input bias current	SNSx = 300 mV		20	**30**	µA
V_{OS}	SNSx amp offset voltage	REFIN = 300 mV (LM3431)	**-5**		**+5**	mV
V_{OS}	SNSx amp offset voltage	REFIN = 300 mV (LM3431A)	**-3**		**+3**	mV
V_{OS_DELTA}	Ch. To Ch. offset voltage mismatch (3)	REFIN = 300 mV, 25°C (LM3431)			5.5	mV
V_{OS_DELTA}	Ch. To Ch. offset voltage mismatch (3)	REFIN = 300 mV, -40°C to +125°C (LM3431)			**6**	mV
V_{OS_DELTA}	Ch. To Ch. offset voltage mismatch (3)	REFIN = 300 mV, 25°C (LM3431A)			3.5	mV
V_{OS_DELTA}	Ch. To Ch. offset voltage mismatch (3)	REFIN = 300 mV, -40°C to +125°C (LM3431A)			**4**	mV
bw	SNSx amp bandwidth	At unity gain		2		MHz
V_{LEDOFF}	LEDOFF voltage	DIM low		5		V
V_{DIM}	DIM threshold	MODE/F > 4V		1.9	**2.3**	V
	hysteresis			0.8		V
T_{DIM}	Minimum internal DIM pulse width (4)			0.4		µs
DIM_{DLY_R}	DIM to NDRV delay time	DIM rising		100		ns
DIM_{DLY_F}	DIM to NDRV delay time	DIM falling		90		ns
$TH_{MODE/F}$	MODE/F threshold	For Digital Dimming control		3.8		V
$I_{MODE/F}$	MODE/F source/sink current			40		uA
V_{MODE_L}	MODE/F minimum voltage	Analog dimming mode		0.37		V
V_{MODE_H}	MODE/F peak voltage	Analog dimming mode		2.5		V

(1) All room temperature limits are 100% production tested. All limits at temperature extremes are specified through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) IQ specifies the current into the VIN pin and applies to non-switching operation.
(3) V_{OS_DELTA} specifies the maximum absolute difference between the offset of any pair of SNS amplifiers.
(4) The minimum DIM pulse width is an internal signal. Any pulse width may be applied to the DIM pin or generated via analog dimming mode. A pulse width less than 0.4 µs will be internally extended to 0.4 µs.

ELECTRICAL CHARACTERISTICS (continued)

Specifications in standard type are for T_J = 25°C only, and limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Unless otherwise stated, V_{IN} = 12V. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
PROTECTION						
V_{SC_SHORT}	SC high threshold	LED short circuit fault, SC rising	**5.7**	6	**6.2**	V
V_{SC_OPEN}	SC open clamp voltage	LED open circuit fault, SC rising	**3.16**	3.50	**3.87**	V
I_{DLY_SC}	DLY source current	DLY = 1.0V	**39**	57	**73**	µA
I_{DLY_SK}	DLY sink current	DLY = 1.0V		1.8		µA
V_{DLY}	DLY threshold voltage	DLY rising	**2.40**	2.8	**3.16**	V
V_{DLY_reset}	DLY reset threshold voltage	DLY falling		350		mV
T_{DLY_BLK}	DLY blank time	DIM rising		1.6		µs
V_{THM}	THM threshold		**1.19**	1.23	**1.27**	V
I_{THM}	THM hysteresis current	THM = 1V		9.6		µA
I_{ILIM}	ILIM max source current	COMP = 2.0V	**31**	40	**46**	µA
V_{AFB_max}	AFB overvoltage threshold		**1.87**	2.0	**2.22**	V
V_{AFB_UVP}	AFB undervoltage threshold	AFB falling	0.73	0.85	0.98	V
T_{SD}	Thermal shutdown threshold			160		°C
BOOST CONTROLLER						
V_{CFB}	CFB voltage	DIM high	1.60	1.71	1.82	V
I_{CFB}	CFB source current	DIM high	35	50	65	µA
CFB_{TC}	CFB temperature coefficient			-2.6		mV/°C
$\Delta V_{CFB} / \Delta V_{IN}$	CFB Line regulation	5.5V < VIN < 36V		0.001		%/V
$I_{SS/SH}$	SS/SH source current	At EN going high	**13**	19	**24**	µA
V_{SS_END}	SS/SH voltage	At end of soft-start cycle	1.80	1.85	1.90	V
V_{RT}	RT voltage	R_{RT} = 34.8 kΩ		1.22		V
F_{SW}	Switching Frequency	R_{RT} = 34.8 kΩ	**651**	700	**749**	kHz
	Minimum Switching Frequency	R_{RT} = 130 kΩ	**180**	200	**220**	
	Maximum Switching Frequency	R_{RT} = 22.6 kΩ	**900**	1000	**1100**	
T_{on_min}	Minimum on time			170	**230**	ns
D_{MAX}	Maximum duty cycle		**80**	85		%
$ILIM_{gm}$	ILIM amplifier transconductance	COMP to ILIM gain		85		umho
Vslope	Slope compensation	Peak voltage per cycle		75		mV
I_{COMP_SC}	COMP source current	VCOMP = 1.2V, AFB = 0.5V		155		µA
I_{COMP_SK}	COMP sink current	VCOMP =1.2V, AFB = 1.5V		150		µA
EA_{gm}	Error amplifier transconductance	CFB to COMP gain, DIM high		230		umho
R_{LG}	Gate Drive On Resistance	Source Current = 200 mA, VIN = 5.5V		6.4		Ω
		Sink Current = 200 mA		2.2		Ω
I_{LG}	Driver Output Current	Source, LG = 2.5V, VIN = 5.5V		0.35		A
		Sink, LG = 2.5V		0.70		A

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_J = 25°C.

V_{REF} vs. Temperature

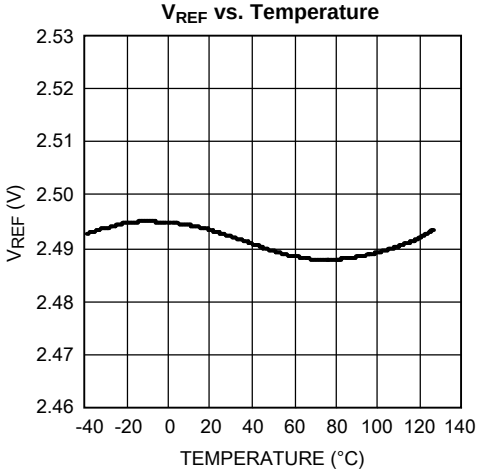


Figure 2.

C_{FB} Voltage vs. Temperature

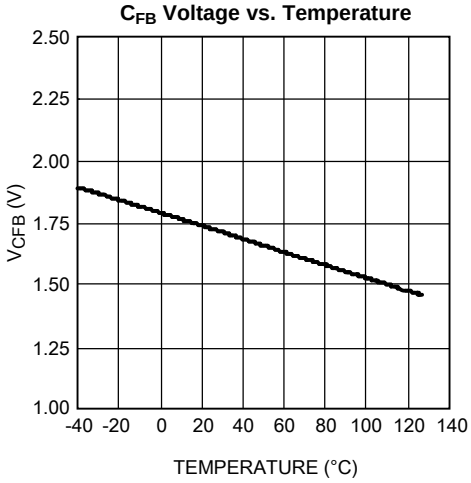


Figure 3.

SNS 1, 2, 3 V_{OS} vs Temperature (LM3431 or LM3431A)

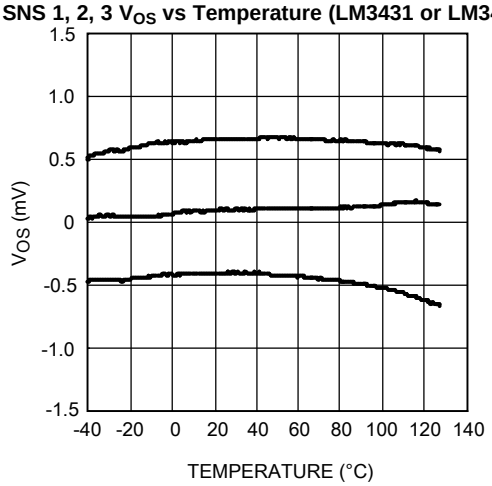


Figure 4.

Delta V_{OS} Max vs Temperature (LM3431 or LM3431A)

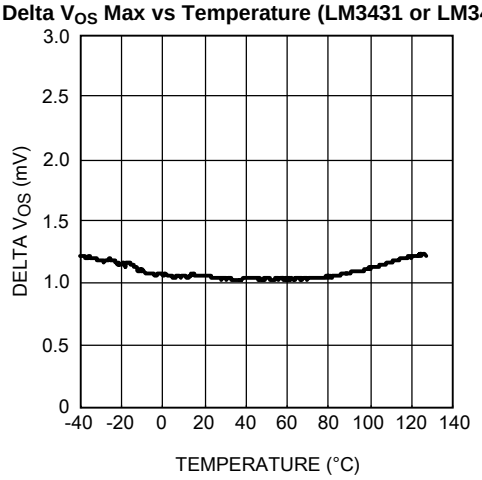


Figure 5.

IQ_SB vs Temperature

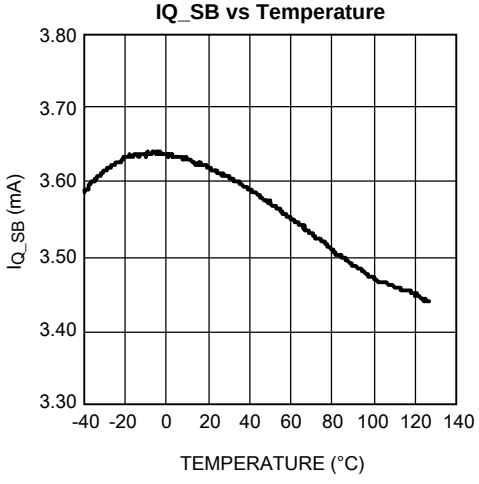


Figure 6.

IQ_SD vs Temperature

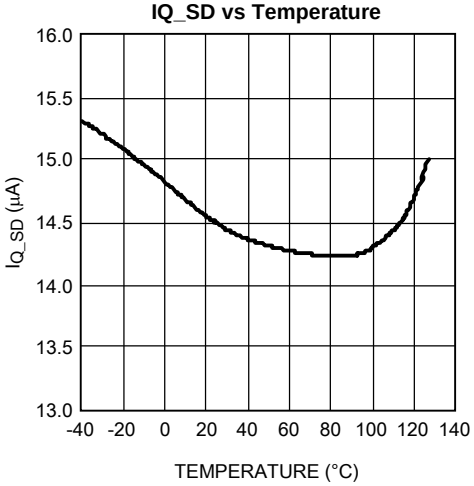


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_J = 25°C.

Normalized Switching Frequency vs. Temperature (700 kHz)

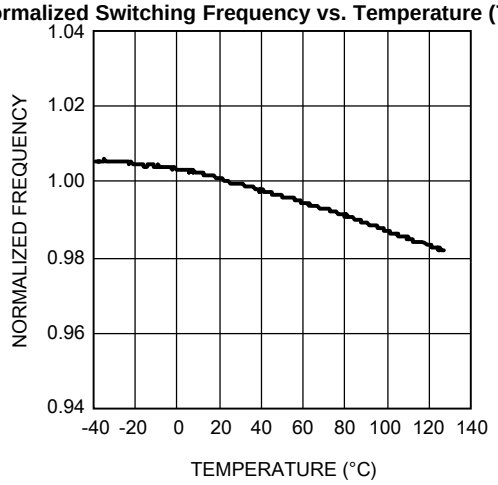


Figure 8.

Efficiency vs. Input Voltage LED Current = 140 mA x 3, LED Vf = 25V

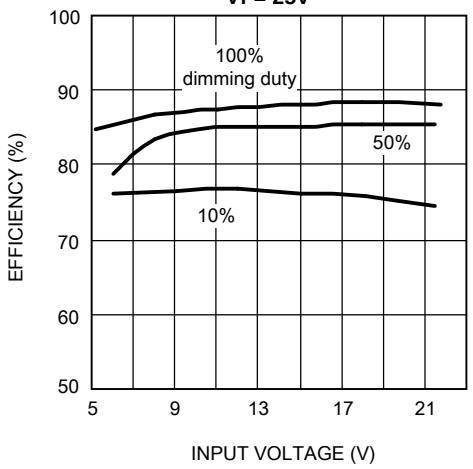


Figure 9.

Line Transient Response

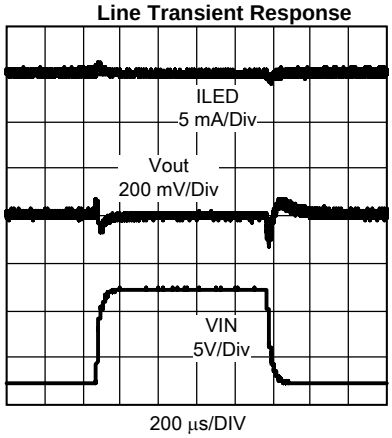


Figure 10.

Dimming Transient Response

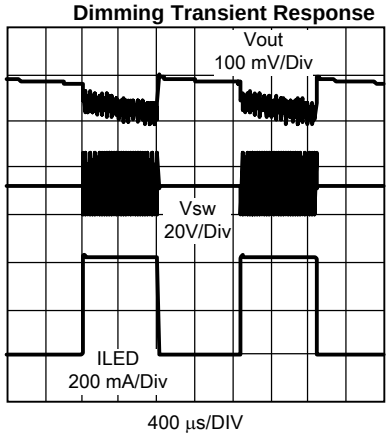


Figure 11.

LED Ripple Current

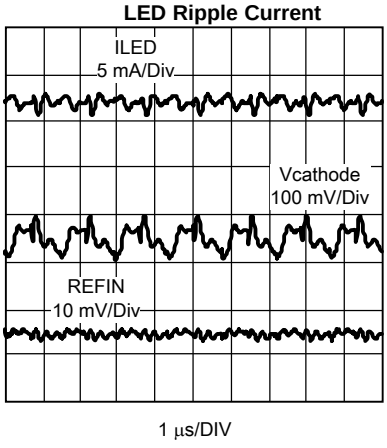


Figure 12.

NDRV Waveforms

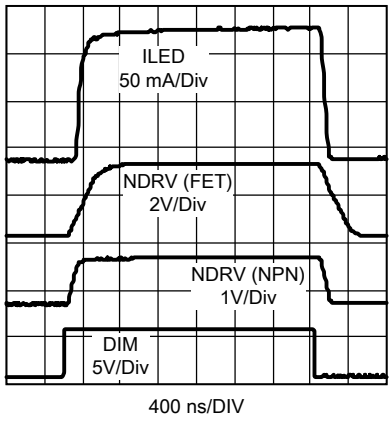
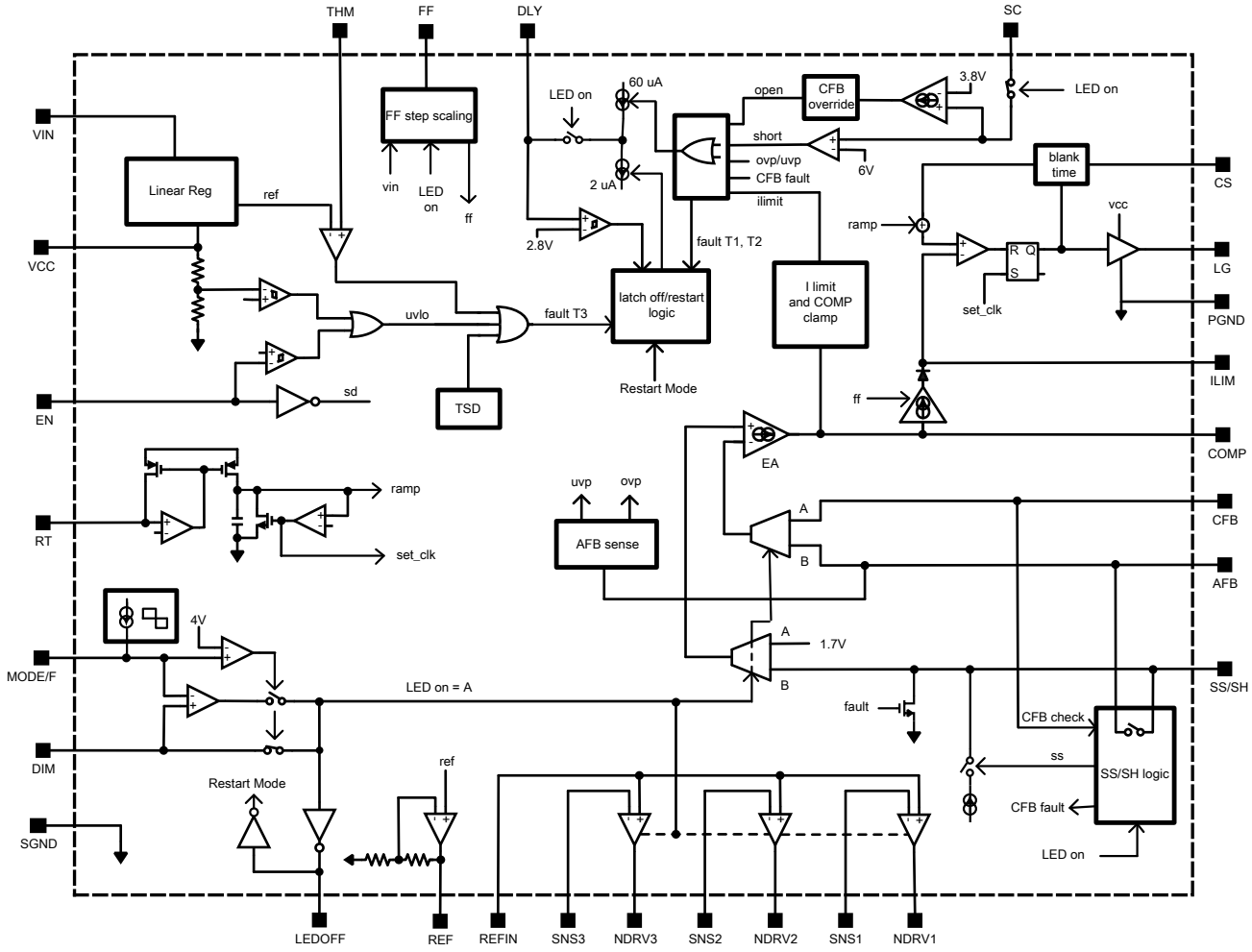


Figure 13.

BLOCK DIAGRAM



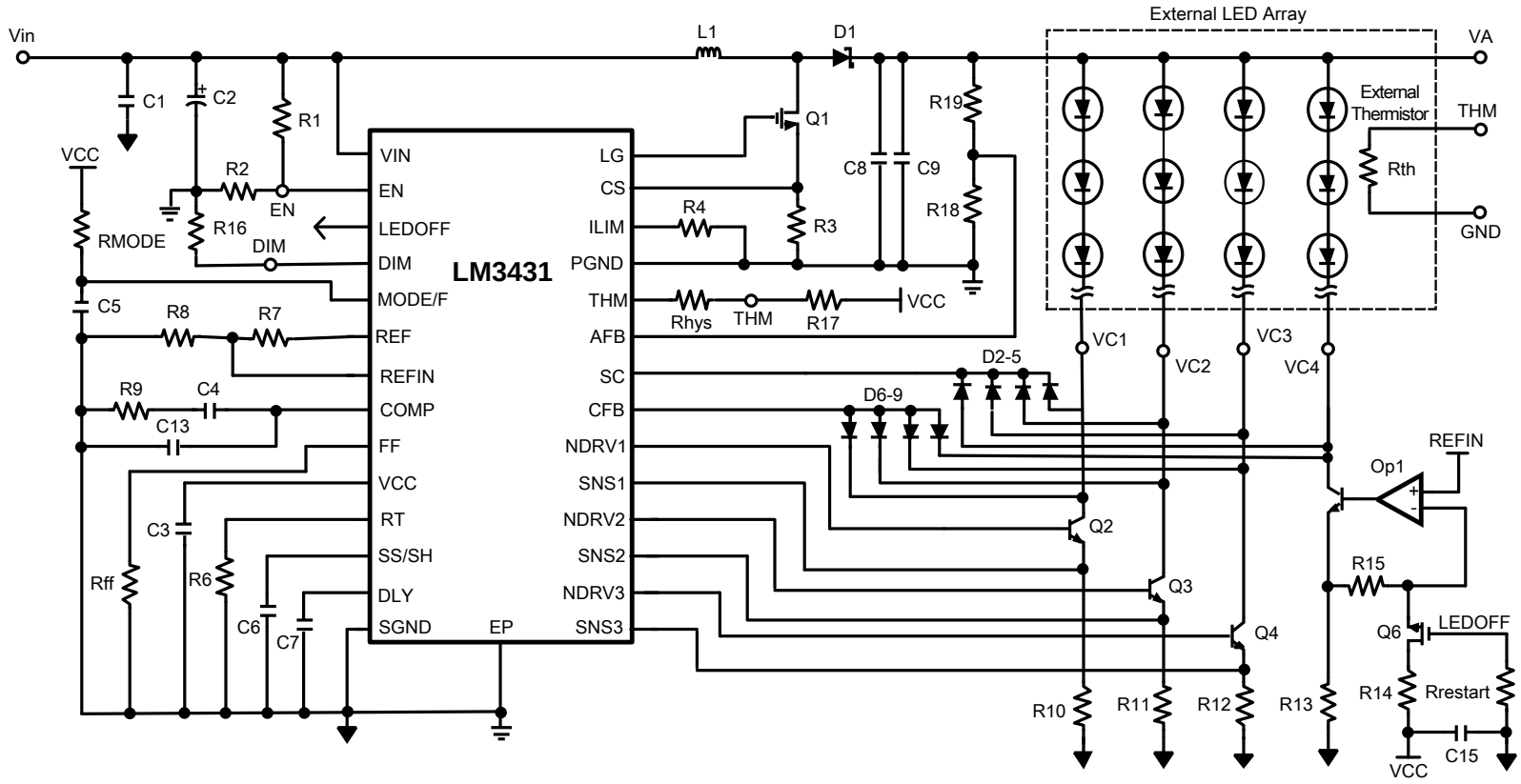


Figure 14. Typical Application Schematic

OPERATION DESCRIPTION

The LM3431 combines a boost controller and 3 constant current regulator controllers in one device. To simplify the description, these two blocks will be described separately as Boost Controller and LED Current Regulator. All descriptions and component numbers refer to the Figure 14 schematic. The LED bottom cathode nodes (VC1 – VC4) are referred to simply as the cathode.

BOOST CONTROLLER

The LM3431 is a current-mode, PWM boost controller. Although the LM3431 may be operated in either continuous or discontinuous conduction mode, the following guidelines are designed for continuous conduction operation. This mode of operation gives lower output ripple and better LED current regulation.

In continuous conduction mode (when the inductor current never reaches zero), the boost regulator operates in two cycles. In the first cycle of operation, the NFET is turned on and current ramps up and is storing energy in the inductor. During this cycle, diode D1 is reverse biased and load current is supplied by the output capacitors - C8 and C9 in Figure 14.

In the second cycle, the NFET is off and the diode is forward biased. Inductor current is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage and is expressed as D or D':

$$D' = 1\text{-}D = \frac{V_{IN}}{V_{OUT}} \tag{1}$$

where D is the duty cycle of the switch.

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{2}$$

Maximum duty cycle is limited to 85% typically.

As input voltage approaches the nominal output voltage, duty cycle and switch on time are reduced. When the on time reaches minimum, pulse skipping will occur. This increases the output ripple voltage and can cause regulator saturation and poor LED current regulation. If input voltage equals or exceeds the set output voltage, switching will stop and the output voltage will become unregulated. This will force an increase in the LED cathode voltage and NPN regulator power dissipation. Although this condition can be tolerated, it is not recommended.

Therefore, input voltage should be restricted to keep on time above the minimum (see Switching Frequency section) and at least 1V below the set output voltage.

ENABLE and UVLO

The EN pin is a dual function pin combining both enable and programmable undervoltage lockout (UVLO). The shutdown threshold is 0.75V. When EN is pulled below this threshold, the LM3431 will shutdown and IQ will be reduced to 15 µA typically. The typical EN pin UVLO threshold is 1.23V. When the EN voltage is above this threshold, the LM3431 will begin softstart. Below the UVLO threshold, the LM3431 will remain in standby mode. A resistor divider, shown as R1 and R2 in Figure 14, can be used to program the UVLO threshold at the EN pin. This feature is used to shutdown the IC at an input voltage higher than the internal VCC UVLO threshold of 4.4V. The EN UVLO should be set just below the minimum input voltage for the application.

The internal UVLO is monitored at the VCC pin. When VCC is below the threshold of 4.4V, the LM3431 is in standby mode (See VCC section).

Soft-Start

The SS/SH pin is a dual function softstart and sample/hold pin. The SH function is described in sections below. When the EN pin is pulled above the programmable UVLO threshold and VCC rises above the internal UVLO threshold, the SS/SH pin begins sourcing current. This charges the SS cap (C6) and the SS pin voltage in turn controls the output voltage ramp-up, sensed via the AFB pin. The softstart capacitor is calculated as shown below, where 20 µA is the typical softstart source current:

$$C6 = \frac{t_{ss} \times 19\ \mu A}{1.85V} \tag{3}$$

The LED current regulators are held off until softstart is completed. During softstart, current limit is active and the CFB pin is monitored for a cathode short fault (See LED Protection section). When the SS/SH voltage reaches 1.85V, the current regulators are activated, LED current begins flowing, and output voltage control is transferred to the CFB pin. Typical startup is shown below in Figure 15.

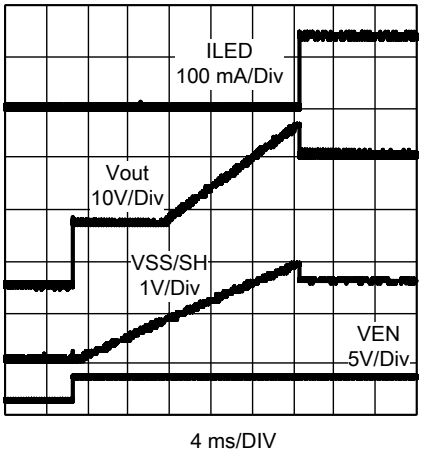


Figure 15. Typical Startup Waveforms (From power-on, DIM = high)

Output Voltage, OVP, and SH

The LM3431 boost controls the LED cathode voltage in order to drive the LED strings with sufficient headroom at optimum efficiency. When the LED strings are on, voltage is regulated to 1.7V (typical) at the CFB pin, which is one diode Vf above the LED cathode voltage. Therefore, when the LED strings are on, the output voltage (LED anodes, shown as VA in Figure 14) will vary according to the Vf of the LED string, while the LED cathode voltage will be regulated via the CFB pin.

The AFB pin is used to regulate the output voltage when the LED strings are off, which is during startup and dimming off cycles. During LED-off times, the cathode voltage is not regulated.

AFB should set the initial output voltage to at least 1.0V (CFB voltage minus one diode drop) above the maximum LED string forward voltage. This ensures that there is enough headroom to drive the LED strings at startup and keeps the SS/SH voltage below its maximum. The AFB pin voltage at the end of softstart is 1.85V typically, which determines the ratio of the feedback resistors according to the following equation:

$$R19 = R18 \times = \frac{V_{OUT(MAX)} - 1.85V}{1.85V} \tag{4}$$

The AFB resistors also set the output over-voltage (OVP) threshold. The OVP threshold is monitored during both LED on and LED off states and protects against any over voltage condition, including all LEDs open (See Open LED section).The OVP threshold at Vout can be calculated as follows:

$$V_{OVP} = \frac{2.0 \times (R19 + R18)}{R18} \tag{5}$$

Because OVP has a fixed 2.0V threshold sensed at AFB, a larger value for R19 will increase the OVP threshold of the output voltage. During an open LED fault, the output voltage will increase by 2.6V typically (see LED Protection section). Therefore, at least this much headroom above the nominal output voltage is required to avoid a false OVP error. Note that because of the high output voltage setting at the end of softstart, a brief open LED error may occur during the short time it takes for the cathode voltage to drop to its nominal level. Figure 15 shows a typical startup waveform, where both Vout and the SS/SH voltage reach their peak before the LED current turns on. Once LED current starts, SS/SH and Vout drop to the nominal operating point.

While the LEDs are on, the AFB voltage is sampled to the SS/SH pin. During LED-off time, this SS/SH voltage is used as the reference voltage to regulate the output. This allows the output voltage to remain stable between on and off dimming cycles, even though there may be wide variation in the LED string forward voltage. The SS/SH pin has a maximum voltage of 1.9V. Therefore, the AFB voltage when the LEDs are on must be below this limit for proper regulation. This will be ensured by setting the AFB resistors as described above. During LED-off cycles, there is minimal loading on the output, which forces the boost controller into pulse skipping mode. In this mode, switching is stopped completely, or for multiple cycles until the AFB feedback voltage falls below the SS/SH reference level.

Switching Frequency

The switching frequency can be set between 200 kHz and 1 MHz with a resistor from the RT pin to ground. The frequency setting resistor (R6 in Figure 14) can be determined according to the following empirically derived equation:

$$R_T = 35403 \times f_{SW}^{-1.06} \quad (6)$$

Where

- f_{SW} is in kHz
- the R_T result is in kohm.

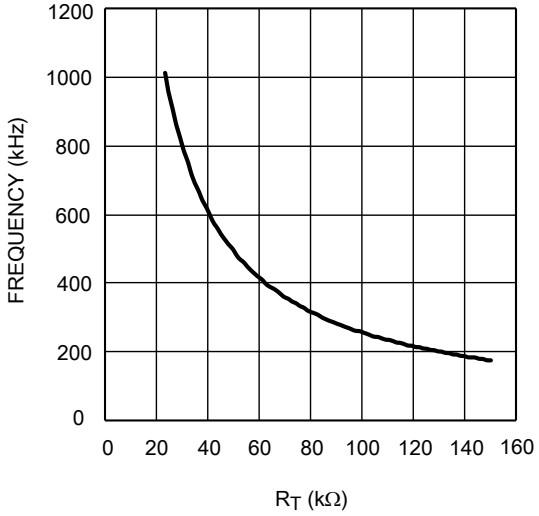


Figure 16. Switching Frequency vs R_T

For a given application, the maximum switching frequency is limited by the minimum on time. When the LM3431 reaches its minimum on-time, pulse skipping will occur and output ripple will increase. To avoid this, set the operating frequency below the following maximum setting:

$$f_{SW(MAX)} = \frac{D}{t_{ON(MIN)}} \quad (7)$$

Inductor Selection

Figure 17 shows how the inductor current, I_L, varies during a switching cycle.

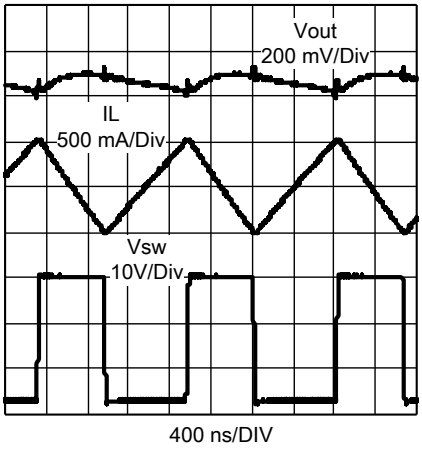


Figure 17. Inductor Current, SW Voltage, and V_{OUT}

The important quantities in determining a proper inductance value are $I_{L(AVE)}$ (the average inductor current) and Δi_L (the peak to peak inductor current ripple). If Δi_L is larger than 2 x $I_{L(AVE)}$, the inductor current will drop to zero for a portion of the cycle and the converter will operate in discontinuous conduction mode. If Δi_L is smaller than 2 x I_L, the inductor current will stay above zero and the converter will operate in continuous conduction mode.

To determine the minimum L, first calculate the $I_{L(AVE)}$ at both minimum and maximum input voltage:

$$I_{L(AVE)} = \frac{I_{OUT}}{D'} \quad (8)$$

Where

- I_{OUT} is the sum of all LED string currents at 100% dimming

$I_{L(AVE)}$ will be highest at the minimum input voltage. Then determine the minimum L based on Δi_L with the following equation:

$$L_{(MIN)} = \frac{V_{IN(MAX)} \times D_{(MIN)}}{\Delta i_L \times f_{SW}} \quad (9)$$

A good starting point is to set Δi_L to 150% of the minimum $I_{L(AVE)}$ and calculate using that value. The maximum recommended Δi_L is 200% of $I_{L(AVE)}$ to maintain continuous current in normal operation. In general a smaller inductor (higher ripple current) will give a better dimming response due to the higher dI/dt. This is shown graphically below.

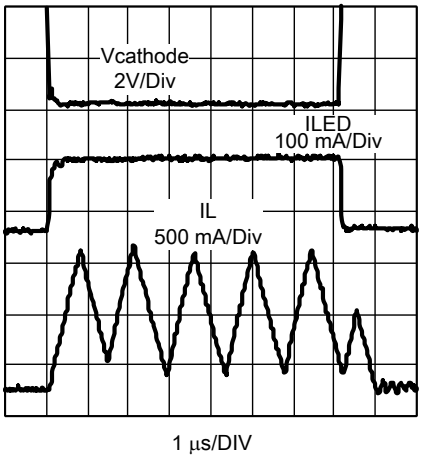


Figure 18. Inductor Current During Dimming

The resulting peak to peak inductor current is:

$$\Delta i_L = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (10)$$

And the resulting peak inductor current is:

$$IL_{PEAK} = IL_{(AVE)} + \frac{\Delta i_L}{2} \quad (11)$$

Peak inductor current will occur at minimum V_{IN}.

The inductor must be rated to handle both the average current and peak current, which is the same as the peak switch current. As switching frequency increases, less inductance is required. However, some minimum inductance value is required to ensure stability at duty cycles greater than 50%. The minimum inductance required for stability can be calculated as:

$$L_{(MIN)} = \frac{R3 \times (V_{OUT} - 2 \times VIN_{(MIN)})}{f_{SW} \times 75\ mV \times 2} \quad (12)$$

Where

- R3 is the sense resistor determined in the next section.

Although the inductor must be large enough to meet both the stability and the Δi_L requirements, a value close to minimum will typically give the best performance.

Current Sensing

Switch current is sensed via the sense resistor, R3, while the switch is on and the inductor is charging. The sensed current is used to control switching and to monitor current limit. To optimize the control signal, a typical sense voltage between 50mV and 200mV is recommended. The sense resistor can therefore be calculated by the following equation:

$$\frac{50\ mV}{IL_{(AVE\_MIN)}} \le R3 \le \frac{200\ mV}{IL_{(AVE\_MAX)}} \quad (13)$$

Since $I_{L(AVE)}$ will vary with input voltage, R3 should be determined based on the full input voltage range, although the resulting value may extend somewhat outside the recommended range.

Current Limit

Current limit occurs when the voltage across the sense resistor (measured at the CS pin) equals the current limit threshold voltage. The current limit threshold is set by R4. This value can be calculated as follows:

$$R4 = \frac{(IL_{(LIM)} \times R3) + (D \times 75\ mV)}{40\ \mu A} \quad (14)$$

Where 40 µA is the typical ILIM source current in current limit and ILlim is the peak (not average) inductor current which triggers current limit.

To avoid false triggering, current limit should be set safely above the peak inductor current level. However, the current limit resistor also has some effect on the control loop as seen in the block diagram. For this reason, R4 should not be set much higher than necessary. When current limit is activated, the NFET will be turned off immediately until the next cycle. Current limit will typically result in a drop in output and cathode voltage. This will cause the COMP pin voltage to increase to maximum, which will trigger a fault and start the DLY pin source current (see LED Protection section). The LM3431 will continue to operate in current limit with reduced on-time until the DLY pin has reached its threshold. However, the current limit cannot reduce the on-time below the minimum specification.

In a boost switcher, there is a direct current path between input and output. Therefore, although the LM3431 will shutdown in a shorted output condition, there are no means to limit the current flowing from input to output.

Note that if the maximum duty cycle of 85% (typical) is reached, the LM3431 will behave as though current limit has occurred.

VCC

The VCC pin is the output of the internal voltage regulator. It must be bypassed to PGND with a minimum 4.7 µF ceramic capacitor. Although VCC is capable of supplying up to 72 mA, external loads will increase the power dissipation and temperature rise within the LM3431. See the TSD section for more detail. Above 72 mA, the VCC voltage will drop due to current limit. Since the UVLO threshold is monitored at this pin, UVLO may be enabled by a VCC over current event.

For input voltages between 4.5V and 5.5V, connect VCC to V_{IN} through a 4.7Ω resistor. This will hold VCC above the UVLO threshold and allow operation at input voltages as low as 4.5V. It may also be necessary to add additional V_{IN} and VCC capacitance for low V_{IN} operation.

Diode Selection

The average current through D1 is the average load current (total LED current), and the peak current through the diode is the peak inductor current. Therefore, the diode should be rated to handle more than the peak inductor current which was calculated earlier. The diode must also be capable of handling the peak reverse voltage, which is equal to the output voltage (LED Anode voltage). To improve efficiency, a low Vf Schottky diode is recommended. Diode power loss is calculated as:

$$P_{DIODE} = Vf \times I_{OUT} \quad (15)$$

NFET Selection

The drive pin of the LM3431 boost switcher, LG, must be connected to the gate of an external NFET. The NFET drain is connected to the inductor and the source is connected to the sense resistor. The LG pin will drive the gate at 5V typically.

The critical parameters for selection of a MOSFET are:

1. Maximum drain current rating, $I_{D(MAX)}$
2. Maximum drain to source voltage, $V_{DS(MAX)}$
3. On-resistance, $R_{DS(ON)}$
4. Total gate charge, Q_g

In the on-state, the switch current is equal to the inductor current. Therefore, the maximum drain current, I_D, must be rated higher than the current limit setting. The average switch current ($_{ID(AVE)}$) is given in the equation below:

$$I_{D(AVE)} = I_{L(AVE)} \times D \quad (16)$$

The off-state voltage of the NFET is approximately equal to the output voltage plus the diode Vf. Therefore, $V_{DS(MAX)}$ of the NFET must be rated higher than the maximum output voltage. The power losses in the NFET can be separated into conduction losses and switching losses. The conduction loss, Pcond, is the I^2R loss across the NFET. The maximum conduction loss is given by:

$$P_{COND} = R_{DS(ON)} \times D_{MAX} \times I_{L(AVE)}^2$$

where

- D_{MAX} is the maximum duty cycle for the given application
- $R_{DS(ON)}$ is the on resistance at high temperature (17)

wThe switching losses can be roughly calculated by the following equation:

$$P_{SW} = \frac{f_{SW} \times IL_{(AVE)} \times V_{OUT} \times (t_{ON} + t_{OFF})}{2}$$

Where

- t_{ON} and t_{OFF} are the NFET turn-on and turn-off times. (18)

Power is also consumed in the LM3431 in the form of gate charge losses, P_g. These losses can be calculated using the formula:

$$P_g = f_{SW} \times Q_g \times V_{IN}$$

where

- Q_g is the NFET total gate charge (19)

Pg adds to the total power dissipation of the LM3431 (See TSD section).

Fast switching FETs can cause noise spikes at the SW node which may affect performance. To reduce these spikes a drive resistor up to 10Ω can be placed between LG and the NFET gate.

Input Capacitor Selection

Because the inductor is at the input of a boost converter, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees relatively low ripple currents. The rms current in the input capacitor is given by:

$$I_{RMS\_IN} = \frac{\Delta i_L}{\sqrt{12}} \tag{20}$$

The input capacitor must be capable of handling this rms current. Input ripple voltage increases with increasing ESR as well as decreasing input capacitance. A typical value of 10 µF will work well for most applications. For low input voltages, additional input capacitance may be required to prevent tripping the UVLO. Additionally, a ceramic capacitor of 1 µF or larger should be placed close to the VIN pin to prevent noise from interfering with normal device operation.

Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the switch is on and the inductor is charging. As a result, the output capacitor sees relatively large ripple currents. The output capacitor must be capable of handling more than the rms current, which can be estimated as:

$$I_{RMS\_OUT} = \sqrt{D' \times \left[I_{OUT}^2 \times \frac{D}{D'^2} + \frac{\Delta iL^2}{12} \right]} \tag{21}$$

Additionally, the ESR of the output capacitor affects the output ripple and has an effect on transient response during dimming. For low output ripple voltage, low ESR ceramic capacitors are recommended. Although not a critical parameter, excessive output ripple can affect LED current.

The output capacitance requirement is somewhat arbitrary and depends mostly on dimming frequency. Although a minimum value of 4 µF is recommended, at lower dimming frequencies, the longer LED-off times will typically require more capacitance to reduce output voltage transients.

When ceramic capacitors are used, audible noise may be generated during LED dimming. Audible noise increases with the amplitude of output voltage transients. To minimize this noise, use the smallest case sizes and if possible, use a larger number of capacitors in parallel to reduce the case size of each. Output transients are also minimized via the FF pin (See Setting FF section). Setting the dimming frequency above 18 kHz or below 500 Hz will also help eliminate the audible effects of output voltage transients.

When selecting an output capacitor, always consider the effective capacitance at the output voltage, which can be less than 50% of the capacitance specified at 0V. Use this effective capacitance value for the compensation calculations below.

Compensation

Once the output capacitor is selected, the control loop characteristics and compensation can be determined. The COMP pin is provided to ensure stable operation and optimum transient performance over a wide range of applications. The following equations define the control-to-output or power stage of the loop:

$$f_{P1} = \frac{KD}{2\pi \times R_L \times C_{OUT}}$$

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$RHP_Z = \frac{V_{OUT} \times (D')^2}{2\pi \times I_{OUT} \times L}$$

$$fpn = \frac{f_{SW}}{2} \tag{22}$$

Where R_L is the load resistance corresponding to LED current, and K_f is calculated as shown:

$$R_L = \frac{V_{OUT}}{I_{OUT}}$$

$$KD = 1 + \frac{D'^2 \times 75\ mV}{I_{OUT} \times R3} + \frac{D'^3 \times R_L}{L \times f_{SW} \times 2} \quad (23)$$

Since the control-to-output response will shift with input voltage, the compensation should be calculated at both the minimum and maximum input voltage.

The zero created by the ESR of the output capacitor, f_{z1}, is generally at a very high frequency if the ESR is small. If low ESR capacitors are used f_{z1} can be neglected and if high ESR capacitors are used, C_{C2} can be added (see below).

A current mode control boost regulator has an inherent right half plane zero, RHPz. This has the effect of a zero in the gain plot, causing a +20dB/decade increase, but has the effect of a pole in the phase, subtracting 90° in the phase plot. This can cause instability if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability, the control loop must be designed to have a bandwidth of less than one third the frequency of the RHP zero. The regulator also has a double pole, fpn, at one half the switching frequency. The control loop bandwidth must be lower than 1/5 of fpn. A typical control-to-output gain response is shown in Figure 19 below.

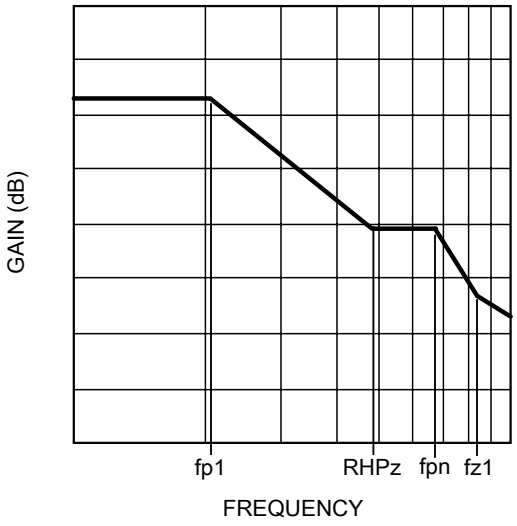


Figure 19. Typical Control-to-Output Bode Plot

Once the control-to-output response has been determined, the compensation components are selected. A series combination of Rc and Cc is recommended for the compensation network, shown as R9 and C4 in the typical application circuit. The series combination of Rc and Cc introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{PC} = \frac{1}{2\pi \times R_O \times C_C}$$

where

- R_O is the output impedance of the error amplifier, approximately 500 kΩ. (24)

The initial value of R_C is determined based on the required crossover frequency from the following equations using the maximum input voltage:

$$R_C = \frac{B}{EA_{gm} \times ILIM_{gm} \times R4}$$

$$B = \frac{f_{CROSS}}{f_{P1} \times A_{cm}}$$

$$A_{cm} = \frac{V_{IN}}{R3 \times I_{OUT} \times KD}$$

Where

- B is the mid-frequency compensation gain (in v/v)
- R4 is the current limit setting resistor
- Acm is the control-output DC gain
- the gm values are given in the ELECTRICAL CHARACTERISTICS table (25)

Fcross is the maximum allowable crossover frequency, based on the calculated values of f_{pn} and RHPz. Any Rc value lower than the value calculated above can be used and will ensure a low enough crossover frequency. Rc should set the B value typically between 0.01v/v and 0.1v/v (-20db to -40db). Larger values of R_C will give a higher loop bandwidth.

However, because the dynamic response of the LM3431 is enhanced by the FF pin (See Setting FF section) the R_C value can be set conservatively. The typical range for R_C is between 300ohm and 3 kΩ. Next, select a value for Cc to set the compensation zero, f_{zc}, to a frequency greater or equal to the maximum calculated value of f_{p1} (f_{zc} cancels the power pole, f_{p1}). Since an fzc value of up to a half decade above fp1 is acceptable, choose a standard capacitor value smaller than calculated. Confirm that fpc, the dominant low frequency pole in the control loop, is less than 100 Hz and below f_{p1}. The typical range for C_C is between 10 nF and 100 nF. The compensation zero-pole pair is shown graphically below, along with the total control loop, which is the sum of the compensation and output-control response. Since the calculated crossover frequency is an approximation, stability should always be verified on the bench.

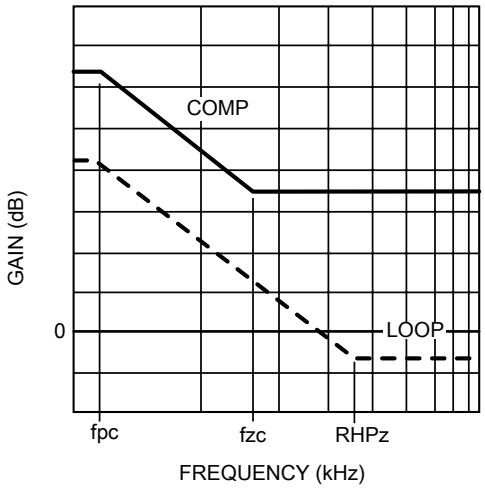


Figure 20. Typical Compensation and Total Loop Bode Plots

When using an output capacitor with a high ESR value, another pole, f_{pc2}, may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C2}, shown as C13 in the Figure 14. The pole should be placed at the same frequency as f_{z1}. This pole can be calculated as:

$$f_{PC2} = \frac{1}{2\pi \times C_{C2} \times (R_C \,//\, R_O)} \quad (26)$$

To ensure this equation is valid, and that C_{C2} can be used without negatively impacting the effects of R_C and C_C, f_{pc2} must be at least 10 times greater than f_{zc}.

LED CURRENT REGULATOR

Setting LED Current

LED current is independently regulated in each of 3 strings by regulating the voltage at the SNS pins. Each SNS pin is connected to a sense resistor, shown in the typical application schematic as R10 - R13. The sense resistor value is calculated as follows:

$$R_{SNS} = \frac{REFIN}{I_{LED} + I_{NDRV}} \quad (27)$$

Where

- I_{LED} is the current in each LED string
- REF_{IN} is the regulated voltage at the REFIN pin
- INDRV is the NPN base drive current

If using NFETs, INDRV can be ignored. A minimum REFIN voltage of 100 mV is required, and 200mV to 300mV is recommended for most applications. The REFIN voltage is set with a resistor divider connected to the REF pin, shown as R7 and R8 in the typical application schematic. The resistor values are calculated as follows:

$$R7 = R8 \times \frac{2.5V - REFIN}{REFIN} \quad (28)$$

The sum of R7 and R8 should be approximately 100k to avoid excessive loading on the REF pin.

NDRV

The NDRV pins drive the base of the external NPN or N-channel MOSFET current regulators. Each pin is capable of driving up to 15 mA of base current typically. Therefore, NPN devices with sufficient gain must be selected. The required NDRV current can be calculated from the following equation, where β is the NPN transistor gain.

$$I_{NDRV} = \frac{I_{LED}}{\beta} \quad (29)$$

If NFETs are used, the NDRV current can be ignored. NPN transistors should be selected based on speed and power handling capability. A fast NPN with short rise time will give the best dimming response. However, if the rise time is too fast, some ringing may occur in the LED current. This ringing can be improved with a resistor in series with the NDRV pins. The NPNs must be able to handle a power equal to I_{LED} x NPN voltage. Note that the NPN voltage can be as high as approximately 5.5V in a fault condition. The NDRV pins have a limited slew rate capability which can increase the turn-on delay time when driving NFETs. This delay increases the minimum dimming on-time and can affect the dimming linearity at high dimming frequencies. Low V_{GS} threshold NFETs are recommended to ensure that they will turn fully on within the required time. At dimming frequencies above 10 kHz, NPN transistors are recommended for the best performance.

CFB and SC Diodes

The bottom of each LED string is connected to the CFB and SC pins through diodes as shown in Figure 14. The CFB pin receives voltage feedback from the lowest cathode voltage. The other string cathode voltages will vary above the regulated CFB voltage. The actual cathode voltage on these strings will depend on the LED forward voltages. This ensures that the lowest cathode voltage (highest Vf) will be regulated with enough headroom for the NPN regulator. The SC pin monitors for LED fault conditions and limits the maximum cathode voltage (See LED Protection section). In this way, each LED string's cathode is maintained within a window between minimum headroom and fault condition.

Both the CFB and SC diodes must be rated to at least 100 µA, and the CFB diode should have a reverse voltage rating higher than V_{OUT}. With these requirements in mind, it is best to use the smallest possible case size in order to minimize diode capacitance which can slow the LED current rise and fall times.

Dimming

The LM3431 is compatible with both analog and digital LED dimming signals. The MODE/F pin is used to select analog or digital mode. When MODE/F is pulled above 3.8V, digital mode is enabled and a PWM signal up to 25 kHz can be applied to the DIM pin. In this mode, the LED current regulators will be active when DIM is above 2V (typical) and inactive when DIM is pulled below 1.1V (typical). Although any pulse width may be used at the DIM pin, 0.4 µs is the minimum LED on time (in either digital or analog mode). This limits the minimum dimming duty cycle at high dimming frequencies. For example, at 20 kHz, the dimming duty cycle is limited to 0.8% minimum. At lower dimming frequencies, the dimming duty cycle can be much lower and the minimum depends on the application conditions including the FF setting (see Setting FF section). In analog dimming mode, the MODE/F pin is used to set the PWM dimming frequency, and duty cycle is controlled by varying the analog voltage level at the DIM pin. To operate in analog mode, connect a capacitor from MODE/F to ground, shown as C5 in the typical application (without the pull-up resistor installed). The dimming frequency is set according to the following equation:

$$C5 = \frac{40\ \mu A}{2 \times f_{DIM} \times 2.13} \tag{30}$$

In analog mode, the MODE/F pin will generate a triangle wave with a peak of 2.5V and minimum of 0.37V. The DIM pin voltage is compared to the MODE/F voltage to create an internal PWM dimming signal whose duty cycle is proportional to the DIM voltage. When the DIM voltage is above 2.5V, the duty cycle is 100%. Duty cycle will vary linearly with DIM voltage as shown in Figure 21. Typical analog dimming waveforms are shown below in Figure 22.

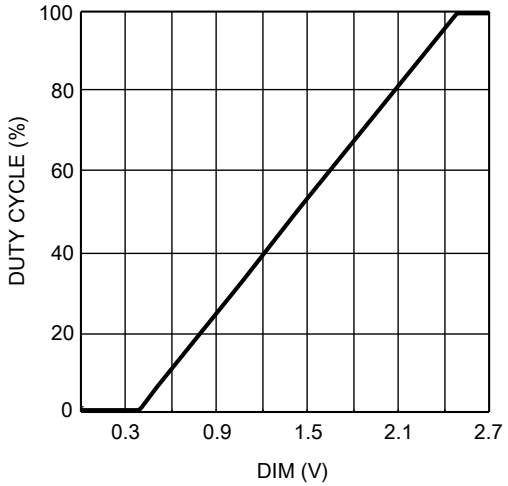


Figure 21. Analog Mode Dimming Duty Cycle vs. DIM voltage

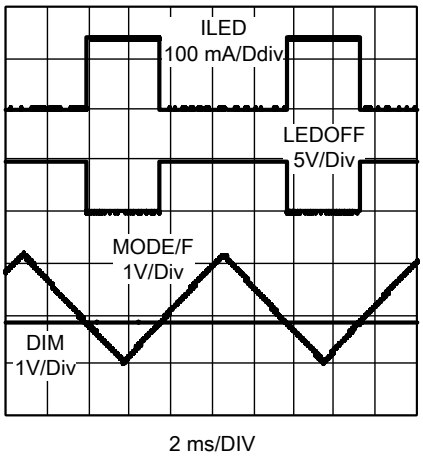


Figure 22. Analog Dimming Mode Waveforms

In PWM dimming, the average LED current is equal to the set LED current (I_{LED}) multiplied by the dimming duty cycle. The average LED current tracks the dimming ratio with exceptional linearity. However, the accuracy of average LED current depends somewhat on the rise and fall times of the external current regulators. This becomes more apparent with short on-times. To ensure good linearity, select NPN regulators with short and similar rise and fall times.

Setting FF

To minimize voltage transients during LED dimming, the output voltage is regulated via the AFB pin during LED off times. However, because the control loop has a limited response time, voltage transients can never be completely eliminated. If these transients are large enough, LED current will be affected and ceramic output capacitors may generate audible noise. The FF pin speeds up the loop response time, and thus minimizes output voltage transients during dimming.

A resistor connected from FF to ground, Rff, sets the FF current which is injected into the control loop at the rising and falling edge of the dimming signal. In this way, the FF pin creates a correction signal before the control loop can respond. A smaller FF resistor will generate a larger correction signal. The minimum recommended Rff value is 10k.

Since the amount of FF correction required for a given application depends on many factors, it is best to determine a FF resistor value through bench testing. Use the following procedure to determine an optimal Rff value:

An Rff value of approximately 20k is a good starting point. A 20 kΩ potentiometer in series with a 10 kΩ resistor works well for bench testing.

The dimming frequency must be selected before setting Rff. Confirm that boost switching operation is stable at 100% dimming duty cycle.

Adjust Rff until the COMP pin voltage is between 0.8V and 0.9V. Next, monitor the cathode voltage response at a low dimming duty cycle while adjusting Rff until the overshoot and undershoot is minimal or there is a slight overshoot.

Check the cathode voltage response at the lowest input voltage and lowest dimming duty cycle and adjust Rff if necessary. This is typically the worst case condition.

The curves in Figure 23 below show the variation in cathode voltage with different Rff settings. Notice that at the ideal setting, both the cathode voltage and COMP voltage are flat. For clarity, the 3 cathode voltage curves in this figure have been offset; all FF settings will result in the cathode voltage settling at 1.2V typically.

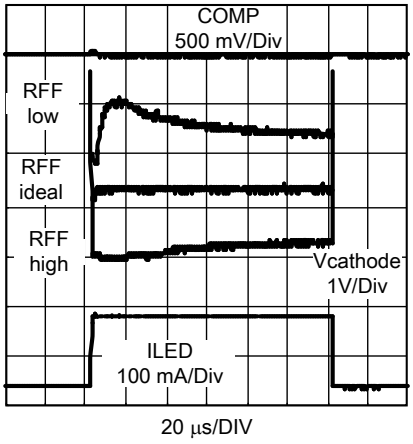


Figure 23. FF Setting Example

Once an Rff value has been set, check the cathode voltage over the input voltage range and dimming duty range. Some further adjustment may be necessary.

In practice the FF pin also has a small effect on the control loop response. As a final step, switching stability at 100% dimming duty should be re-verified once the Rff value has been selected. At the optimal Rff setting, output voltage transients will be minimized and the cathode voltage will be stable across the range of input voltage and dimming duty cycle.

The ideal cathode response illustrated in Figure 23 may not be achievable over the entire input voltage range. However, LED current will not be affected as long as the cathode voltage remains above the regulator saturation voltage and below the open LED fault threshold (See Open LED section).

A wide input voltage range will cause a wider variation in the feedforward effect, thus making duty cycles less than 1% more difficult to achieve. For any given application there is a minimum achievable dimming duty cycle. Below this duty cycle, the cathode voltage will begin to drift higher, eventually appearing as an open LED fault (See LED Protection section).

During an LED open fault condition, cathode voltage overshoot will tend to increase. If Rff is not set appropriately, high overshoots may be detected as an LED short fault and lead to shutdown.

LED Protection

Fault Modes and Fault Delay

The LM3431 provides 3 types of protection against several types of potential faults. Table 1 summarizes the fault protections and groups the fault responses into three types (the auto-restart option is described in the next section).

Table 1. Fault Mode Summary

Fault	Mechanism	Action	Response	Type
1 LED open	SC > 3.1V	DLY charges	continue to regulate	1
1 LED short	SC > 3.1V	DLY charges	continue to regulate	
All LEDs open	AFB > 2.0V	DLY charges	Shutdown or auto-restart	2
Output over-voltage	AFB > 2.0V	DLY charges	Shutdown or auto-restart	
multiple LED short	SC > 6.0V	DLY charges	Shutdown or auto-restart	
Multiple LED short, VIN<6V	AFB < 0.85V	DLY charges	Shutdown or auto-restart	
Cathode short	CFB low at startup	DLY charges	Shutdown or auto-restart	
Current limit	COMP at max	DLY charges	Shutdown or auto-restart	
UVLO	VCC or EN low	No DLY flag	stand by	3
TSD	IC over temperature	No DLY flag	stand by	
THM	THM < 1.2V	No DLY flag	stand by	

When Type 1 or Type 2 faults occur, the DLY pin begins sourcing current (57 µA typical). A capacitor connected from DLY to ground (C7) sets the DLY voltage ramp and shutdown delay time. For a Type 1 fault, the LM3431 will continue to regulate, although the DLY pin remains high. In this condition, the DLY pin will charge to a maximum of 3.6V (typical).

In case of a Type 2 fault, when the DLY voltage reaches 2.8V (typical), the LM3431 will shut down and the DLY pin will remain at 3.6V.

For evaluation and debugging purposes, Type 2 shutdown can be disabled by grounding the DLY pin. It is not recommended to leave the DLY pin open.

For any fault other than a cathode short, the DLY pin will discharge (sinking 1.8 µA) when the fault is removed before shutdown occurs. Since most fault conditions can only be sensed during the LED-on dimming period, the DLY pin will not charge during LED-off times. When the LEDs are off, DLY is in a high impedance state and its voltage will remain constant. If a fault is removed during the LED-off period, DLY will begin discharging at the next LED-on cycle. If the fault is not removed, DLY will continue charging at the next LED-on cycle. Therefore, the DLY charging time is controlled by both the DLY capacitor and the dimming duty cycle. The time for the DLY pin to charge to the shutdown threshold can be calculated as shown:

$$t\_dly = \frac{C7 \times 2.8V}{57\ \mu A} \times \frac{1}{D_{DIM}} \quad (31)$$

Where D_{DIM} is the dimming duty cycle. Figure 24 below shows the DLY pin charging during dimming due to a Type 1 fault:

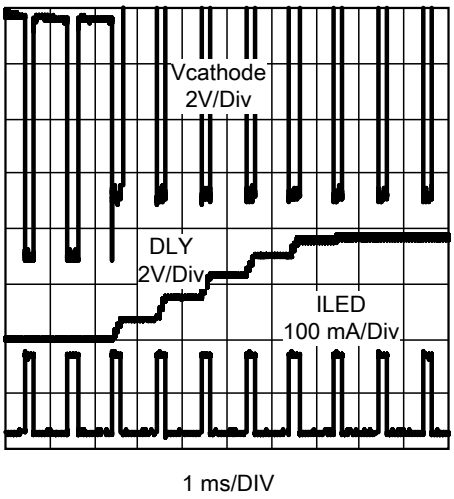


Figure 24. DLY Charging, 1 LED Open Fault

When the LED string turns on, there is a 1.6 µs typical blanking time for fault detection. This ensures that the LED cathode voltage will reach its regulation point and faults will not be falsely triggered. However, faults can not be detected during short dimming cycles of less than 1.6 µs.

When a Type 3 fault occurs, DLY does not charge. The LM3431 will enter standby mode and restart from softstart when the fault condition is removed.

Fault Shutdown and Automatic Restart

In normal operation, the LM3431 must be powered off or put into standby via the EN pin to restart after a fault shutdown. However, the LEDOFF pin can be connected to GND to enable the automatic restart feature. During startup, the LEDOFF voltage is monitored and if grounded, auto-restart mode is enabled.

In auto-restart mode, the DLY pin will be discharged by a 1.8 µA sink current after a Type 2 shutdown. In this mode, DLY will not reach 3.6V, but will start discharging from the shut down threshold of 2.8V. When the DLY pin voltage falls to 350 mV (typical) the LM3431 will restart from softstart mode. In this way, the DLY capacitor controls the restart delay time. If the LEDOFF pin is used to control additional LED strings (see LEDOFF: Adding Additional channels), then the automatic restart feature cannot be enabled.

In the case of an output over-voltage fault (all LEDs open), DLY will not discharge until the AFB voltage falls below the OVP threshold. Figure 25 below shows an OVP fault with auto-restart activated. The output voltage increases when all LEDs are opened, causing DLY to charge. DLY remains at 2.8V until Vout falls below the OVP threshold. When DLY discharges to 350 mV, softstart begins. In auto-restart mode, the LM3431 will re-start continually until the fault is removed. In this example, the fault is removed and normal operation continues after one attempted re-start.

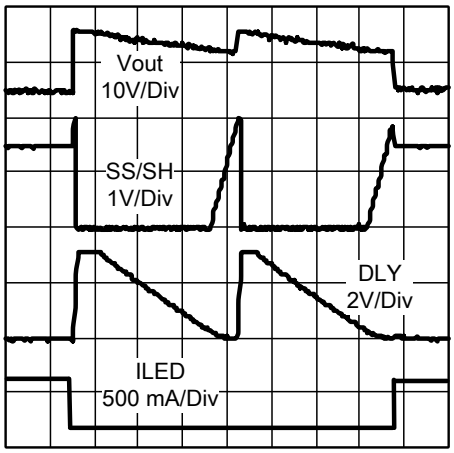


Figure 25. OVP and Auto-Restart

Open LED

If any LED string fails open, the boost regulator will sense a low voltage at the CFB pin. This will cause the output voltage to increase, causing the other LED string cathode voltages to also increase. When the SC pin voltage rises to 3.1V, a Type 1 fault will be triggered and the DLY pin will begin sourcing current. In this mode, the SC voltage will be clamped at 3.5V (typical) and the regulators will continue to operate. At this higher cathode voltage, power dissipation will increase in the external NPN regulators. Power dissipation will also increase in the LM3431 since any open string will cause the NDRV pin to source its maximum current. A one LED open fault condition is shown in Figure 24 above. The open LED causes the cathode voltage to increase, and DLY charges during each LED on cycle while current continues to be regulated in the other LED strings.

If all LED strings fail open, the same action will cause the output voltage to increase. However, in this case, SC will be held low and cannot sense the failure. Instead, this failure mode is sensed by AFB. When AFB reaches its over-voltage threshold of 2.0V (typical), a Type 2 fault will be triggered, the DLY pin will begin sourcing current, and the LM3431 will shut down.

Unlike the SC and CFB fault detection, the AFB pin is always monitored. Therefore, DLY charging time will not be affected by the dimming duty cycle and any over-voltage condition will cause DLY to charge.

Shorted LED

If an LED fails short circuit, the SC voltage will increase. When SC reaches 3.1V, the same Type 1 fault as an open LED will be triggered. Current in the affected string will continue to be regulated, with the cathode clamped at one diode V_f above 3.5V. As in the case of 1 LED open, the power dissipation will increase in the external NPN regulator of the shorted string.

However, if enough LEDs or an entire string are shorted, the SC pin will rise to the short circuit threshold of 6.0V. This will cause a Type 2 fault, and the LM3431 will shut down when the DLY threshold is reached.

When an LED string is shorted, the LM3431 will attempt to reduce the SC voltage to 3.5V. As a result, switching will stop, and the cathode voltage will be brought to the minimum level, which is Vin. If Vin is less than approximately 6V and the DLY time is long enough, SC will fall below the 6V short circuit fault threshold. In this case, the shorted string fault will be detected as an AFB under-voltage (UVP) fault.

When AFB falls below 0.85V (typical) a Type 2 fault will be triggered. As is the case with OVP detection, the AFB UVP threshold is monitored during both LED on and LED off cycles. A UVP fault will cause DLY to charge, unaffected by the dimming duty cycle. Figure 26 below shows the sudden cathode voltage increase due to an LED string short. DLY begins charging and charges continuously when an AFB under-voltage is detected, eventually causing a shutdown.

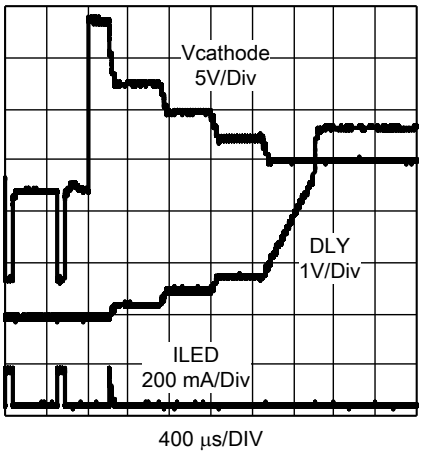


Figure 26. LED String Short Fault and UVP Detection

Shorted Cathode

At the end of softstart, the CFB voltage is monitored. In normal startup, the LED strings are off and CFB voltage increases with the output voltage. If the CFB voltage stays below approximately 1.9V, a cathode short to ground condition is detected and a Type 2 fault is triggered. At the end of soft-start, the DLY pin will begin sourcing current and it will continue sourcing until the shutdown threshold is reached, even if the short condition is removed.

When a cathode short occurs, the LEDs in the affected string will be driven on during the soft-start and DLY periods. Therefore, the DLY and soft-start time should be set short enough for the LED string to withstand the burst of unregulated current.

Thermal Considerations

To optimize performance under all conditions, the LM3431 controls the temperature coefficients of critical parameters and provides over-temperature protection for both the IC and LEDs.

THM

The THM pin is designed to monitor for over-temperature conditions at the LED array. This is done with a negative TC thermistor mounted at the LED panel. The THM circuit is a resistor divider from a reference voltage to ground, shown in Figure 27 as R17 and Rth. As the thermistor temperature increases, the THM pin voltage will decrease. When THM drops to 1.23V (typical), a Type 3 fault is triggered and the LM3431 will enter standby until the thermistor temperature decreases and THM voltage increases. Thermistors are typically specified by their resistance at 25°C, and by their beta constant which describes the temperature coefficient. The resistance value at the desired shutdown temperature can be calculated from the beta constant or found in the thermistor datasheet table. Once the shutdown temperature resistance is known, the R17 value can be calculated as shown below.

$$R17 = Rth @ T \times \frac{VCC - 1.23V}{1.23V} \quad (32)$$

where Rth@T is the thermistor resistance at the desired shutdown temperature. Although VCC is shown in the typical application schematic, any regulated voltage source can be used in its place, including V_{REF}.

In shutdown, THM sinks 10 µA to create some hysteresis. An R17 value of at least 20 kΩ is recommended to create sufficient hysteresis. Larger values of R17 (and Rth) will generate larger hysteresis.

If more hysteresis is required, a resistor can be added in series with THM as shown below:

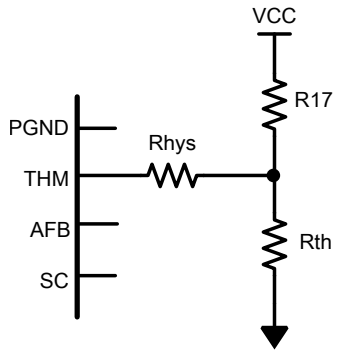


Figure 27. THM Circuit with Hysteresis

The THM hysteresis can be determined by calculating the restart threshold as shown below. If R_{HYS} is not installed, calculate Rth@restart using an R_{HYS} value of 0Ω.

$$\text{Rth @ restart} = \frac{1.23V - (10\ \mu A \times R_{HYS})}{\frac{VCC - 1.23V - (10\ \mu A \times R_{HYS})}{R17}} - 10\ \mu A \quad (33)$$

Where 10 µA is the THM sink current, and Rth@restart is the thermistor resistance at the restart temperature. Refer to the manufacturer datasheet to find the restart temperature at the calculated resistance or use the beta constant to calculate the restart temperature.

During startup (and re-start), the THM monitor is active. Therefore, the thermistor temperature must be below the restart threshold for the LM3431 to startup.

TSD

If the LM3431 internal junction temperature increases above 160°C TSD is activated. This is a Type 3 fault condition. Device temperature rise is determined by internal power dissipation primarily in the LG and NDRVx drivers. The power dissipation can be estimated as follows:

$$P_D = P_{IQ} + P_{NDRV} + P_{VCC} + P_G \quad (34)$$

$$P_{IQ} = V_{IN} \times I_Q$$

Where

- I_Q is 4.0 mA typically (35)

$$P_{NDRV} = (V_{IN} - REFIN - Vbe) \times I_{NDRV} \times D_{DIM} \times \#Strings$$

Where

- REFIN+Vbe is the NDRV voltage
- I_{NDRV} was calculated previously in the NDRV section (36)

For the case of open LEDs, I_{NDRV} on the open string will be at the maximum of 15 mA. The LM3431 power dissipation will be highest in open LED conditions at 100% dimming duty. If NFETs are used for regulation, P_{NDRV} will be a function of dimming frequency and can be calculated as:

$$P_{NDRV\_FET} = f\ dim \times Q_g \times V_{IN} \quad (37)$$

$$P_{VCC} = (V_{IN} - V_{CC}) \times I_{VCC}$$

Where

- $_{VCC}$ is any current being drawn from the VCC pin, such as external op-amp power, or THM voltage divider. (38)

The LG power dissipation, PG is given in the NFET Selection section.

Temperature rise can then be calculated as:

$$T_{RISE} = P_D \times \theta_{JA}$$

Where

- θ_{JA} is typically 32°C/W and varies with pcb copper area (Refer to the PCB Layout section) (39)

Although the TSD threshold is 160°C, the LM3431 may not operate within specification at temperatures above the maximum rating of 125°C. Power dissipation should be limited to ensure that device temperature stays within this limit.

Temperature Coefficients

Several device specifications are designed to vary with temperature. To maintain optimum headroom control and minimum NPN power dissipation, CFB regulation has a tempco of -2.6 mV/°C. This is matched to the typical tempco of the small signal diodes used for the cathode feedback connection. Although the CFB voltage will vary with temperature, the cathode voltage will remain stable. The SS/SH pin rises to 1.85V typically during soft start. This voltage has a tempco of approximately -2.2 mV/°C, which is designed to follow the tempco of the LED strings. At then end of soft start, the anode voltage will be greater than the maximum LED forward voltage, regardless of operating temperature. To avoid false errors, the AFB overvoltage threshold has a tempco of -1.4 mV/°C. Of course, these temperature monitoring features are most effective with the LM3431 mounted within the same ambient temperature as the LEDs.

LEDOFF: Adding Additional channels

Although the LM3431 has three internal current controllers, more channels can easily be added. A fourth LED string is shown in Figure 14 connected to VC4.

For additional channels, the sense resistor should be the same value as the main three channels. During startup and dimming off time, LEDOFF rises to 5V, which quickly turns off the external driver. While the LED strings are on, the LEDOFF signal is low, allowing normal regulation. If LEDOFF is used to add additional channels, it cannot be used to enable auto-restart mode.

All additional channels must also be connected through diodes to the SC and CFB pins as shown in the typical application schematic. The op-amp used to drive the additional channel current regulator must be fast enough to drive the regulator fully on within the DLY blanking time. A slew rate of 5V/µsec is typically sufficient. Also, the op-amp output must be capable of completely turning off the NPN regulator, which requires a drive voltage no greater than the REFIN voltage. A rail-to-rail type op-amp is recommended.

Finally, the R14 resistor should be large enough to limit V_{CC} current during the LED-off cycle. A value of at least 1k is recommended. Any additional channels will have a longer turn-on delay time than channels 1-3. An additional delay time of 250 ns is typical. The added delay can affect dimming linearity at on times less than 1 µs.

LED Current Accuracy

LED string current accuracy is affected by factors both internal and external to the LM3431. For any single string the maximum deviation from ideal is simply the sum of the sense resistor, offset error, REF voltage, REFIN resistor divider accuracy, and bipolar gain variation:

$$\text{Acc\_single\%} = \pm A_{R10} + 2\% + A_{R7} + A_{R8} + \frac{5\text{ mV} \times 100}{\text{REFIN}} + \frac{\Delta\beta \times 100}{2 \times \beta^2} \quad (40)$$

Where

- A_{R10} is the sense resistor % accuracy
- 2% is the REF voltage accuracy, A_{R7}
- A_{R8} are the REFIN setting resistors % accuracy
- 5 mV is the maximum SNS amp offset voltage (use 3 mV for LM3431A)
- β is the gain of NPN transistor
- Δβ is the specified range of gain in the NPN

The string-to-string accuracy is the maximum difference in current between any two strings. It is best calculated using the RSS method:

$$\text{Acc\_s-s\%} = \pm\sqrt{2 \times A_{R10}^2 + \left(\frac{\Delta\beta \times 100}{2 \times \beta^2}\right)^2} + \frac{6\text{ mV} \times 100}{\text{REFIN}} \quad (41)$$

Where

- 6 mV is the maximum SNS amp delta offset voltage (V_{OS_DELTA} over temperature, use 4 mV for LM3431A) and we are assuming the sense resistors have the same accuracy rating

If FETs are used, the β term can be ignored in both equations. The LED current in each string will be within ±Acc_single% of the set current. And the difference between any two strings will be within ±Acc_s-s% of each other.

PCB Layout

Good PCB layout is critical in all switching regulator designs. A poor layout can cause EMI problems, excess switching noise, and improper device operation. The following key points should be followed to ensure a quality layout.

Traces carrying large AC currents should be as wide and short as possible to minimize trace inductance and associated noise spikes.

These areas, shown hatched in Figure 28, are:

- The connection between the output capacitor and diode
- The PGND area between the output capacitor, R3 sense resistor, and bulk input capacitor
- The switch node

The current sensing circuitry in current mode controllers can be easily affected by switching noise. Although the LM3431 imposes 170ns of blanking time at the beginning of every cycle to ignore this noise, some may remain after the blanking time. Following the important guidelines below will help minimize switching noise and its effect on current sensing.

As shown in Figure 28, ground the output capacitor as close as possible to the bottom of the sense resistor. This connection should be somewhat isolated from the rest of the PGND plane (place no ground plane vias in this area). The V_{OUT} side of the output capacitor should be placed close to the diode.

The SW node (the node connecting the diode anode, inductor, and FET drain) should be kept as small as possible. This node is one of the main sources for radiated EMI. Sensitive traces should not be routed in the area of the SW node or inductor.

The CS pin is sensitive to noise. Be sure to route this trace away from the inductor and the switch node. The CS, LG, and ILIM traces should be kept as short as possible. As shown below, R4 must be grounded close to the ground side of R3.

The VCC capacitor should be placed as close as possible to the IC and grounded close to the PGND pin. Take care in routing any other VCC traces away from noise sources and use decoupling capacitors when using VCC as an external voltage supply.

A ceramic input capacitor must be connected as close as possible to the VIN pin and grounded close to the PGND pin.

An isolated ground area shown as SGND is recommended for small signal ground connections. The SGND plane should connect to both the exposed pad (EP) and SGND pin. The SGND and PGND ground planes should be connected to their respective pins and both pins should be connected only through the exposed pad, EP.

Components connecting all of the following pins should be placed close to the device and grounded to the SGND plane: REF, REFIN, AFB, COMP, RT, FF, MODE/F, and SS/SH. These components and their traces should not be routed near the switch node or inductor. The LED current sense resistors should be grounded to the SGND plane for accurate current sensing. This area, shown as LGND in Figure 28, should be somewhat separated from SGND and must provide enough copper area for the total LED current.

If driving more than 3 channels, the layout of the additional channels should be within a minimal area with short trace lengths. This will help to reduce ringing and delay times. Connections to the LED array should be as short as possible. Less than 25 cm is recommended. Longer lead lengths can cause excessive ringing or oscillation.

A large, continuous ground plane should be placed as an inner or bottom layer for thermal dissipation. This plane should be considered as a PGND area and not used for SGND connections. To optimize thermal performance, multiple vias should be placed directly below the exposed pad to increase heat flow into the ground plane. The recommended number of vias is 10-12 with a hole diameter between 0.20 mm and 0.33 mm. See TI Lit Number SNVA183 for more information.

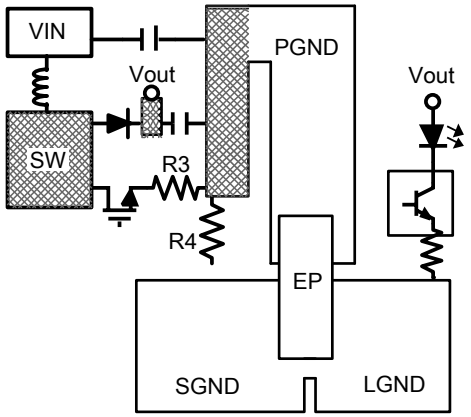


Figure 28. Example PCB Layout

REVISION HISTORY

Changes from Revision F (May 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	29

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3431AMH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431AMH	Samples
LM3431AMHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431AMH	Samples
LM3431AQMH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431 AQMH	Samples
LM3431AQMHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431 AQMH	Samples
LM3431MH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431MH	Samples
LM3431MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431MH	Samples
LM3431QMH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431 QMH	Samples
LM3431QMHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3431 QMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM3431, LM3431-Q1 :

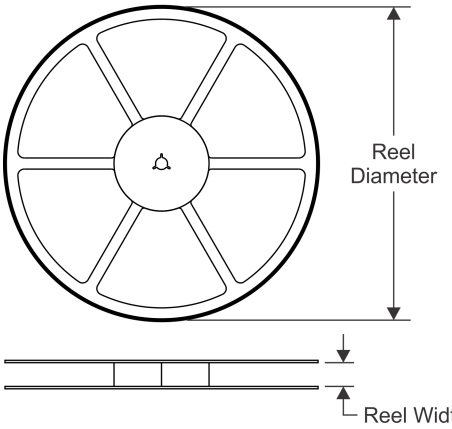
- Catalog: LM3431
- Automotive: LM3431-Q1

NOTE: Qualified Version Definitions:

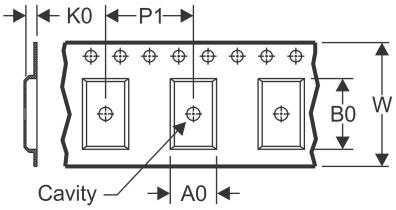
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

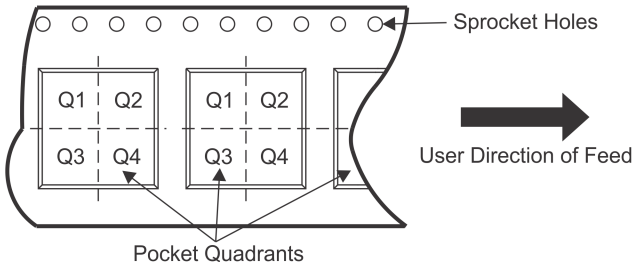


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

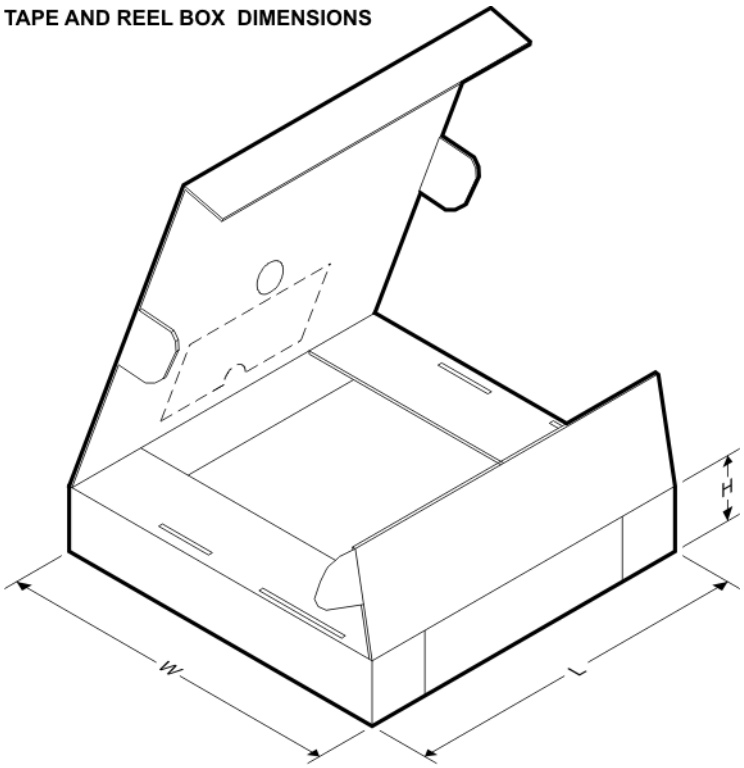
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3431AMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM3431AQMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM3431MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM3431QMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

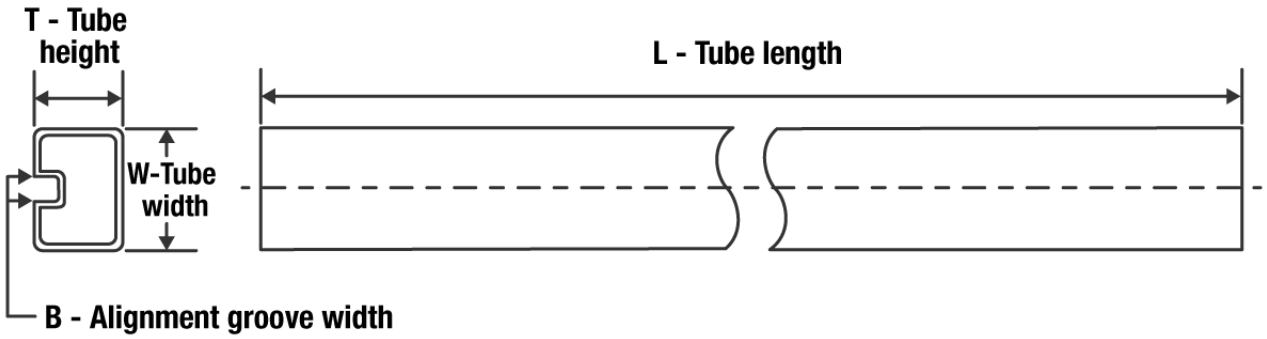
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3431AMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0
LM3431AQMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0
LM3431MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0
LM3431QMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

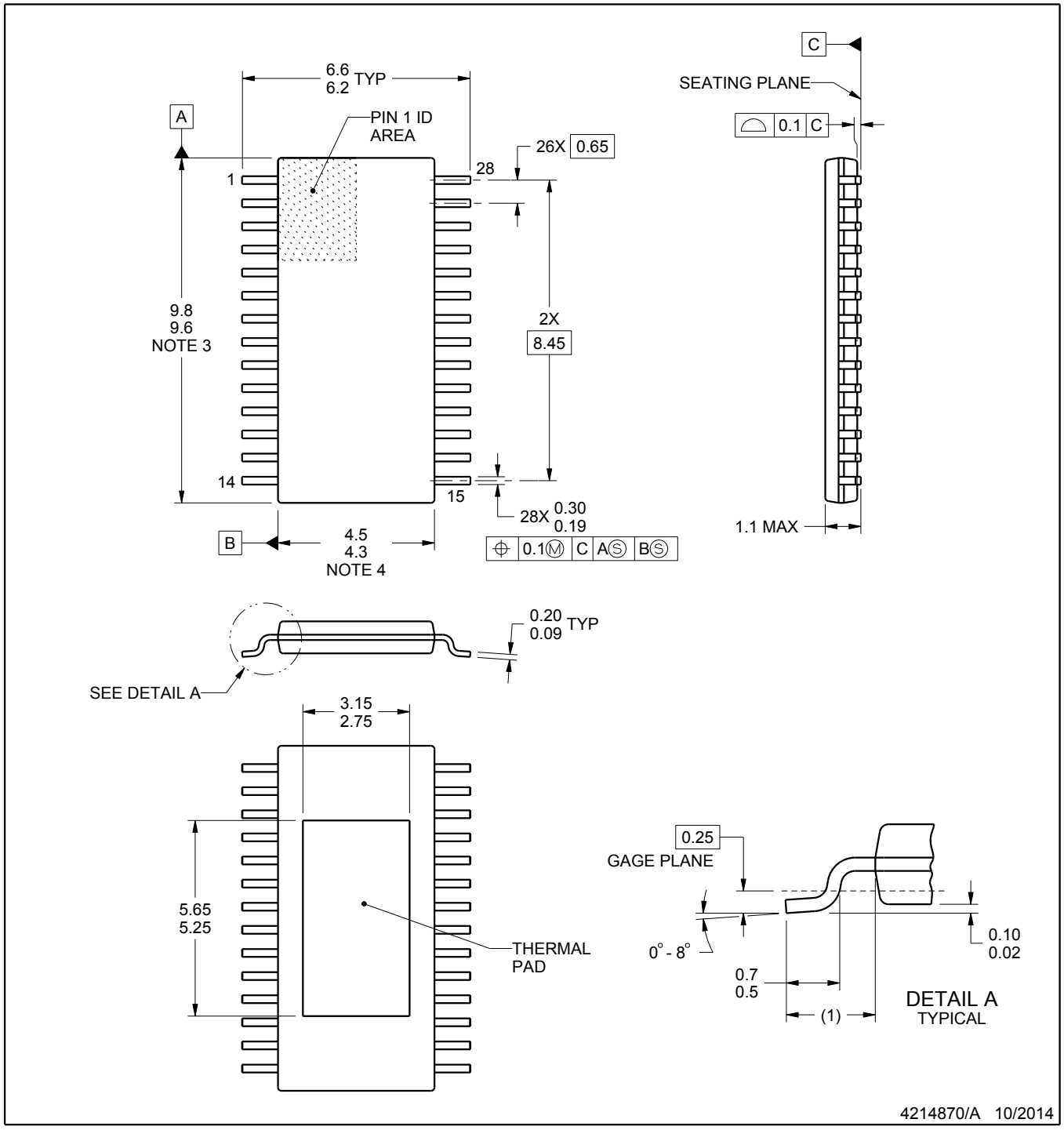
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3431AMH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM3431AQMH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM3431MH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM3431QMH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06

PACKAGE OUTLINE

PWP0028A

PowerPAD™ - 1.1 mm max height

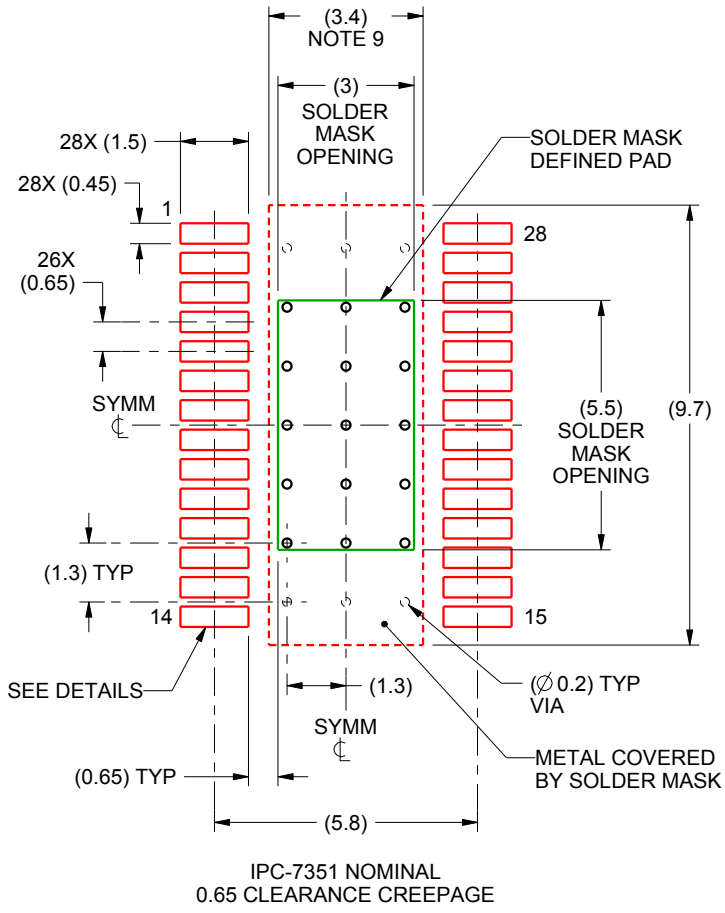
PLASTIC SMALL OUTLINE



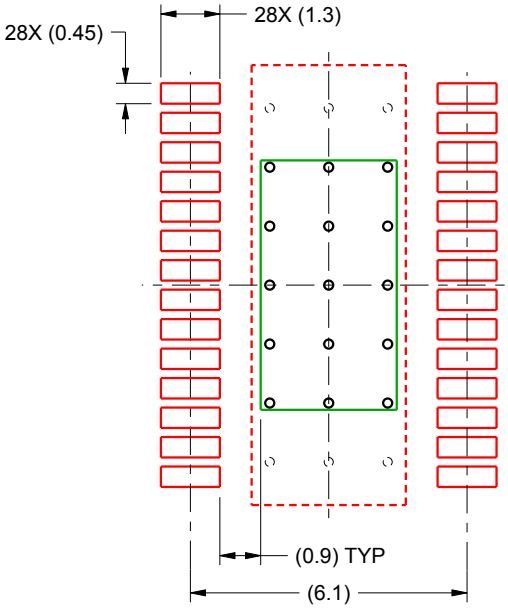
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

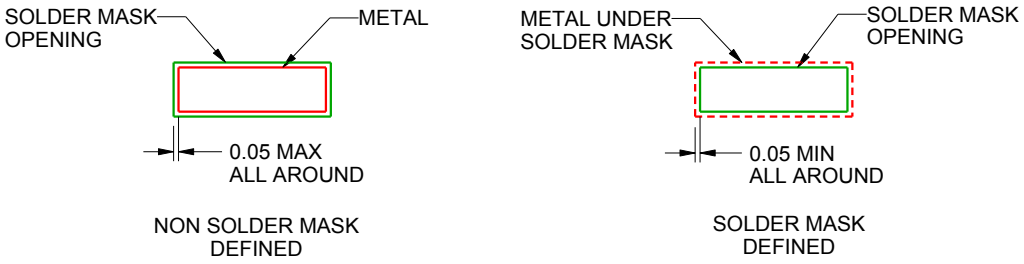


IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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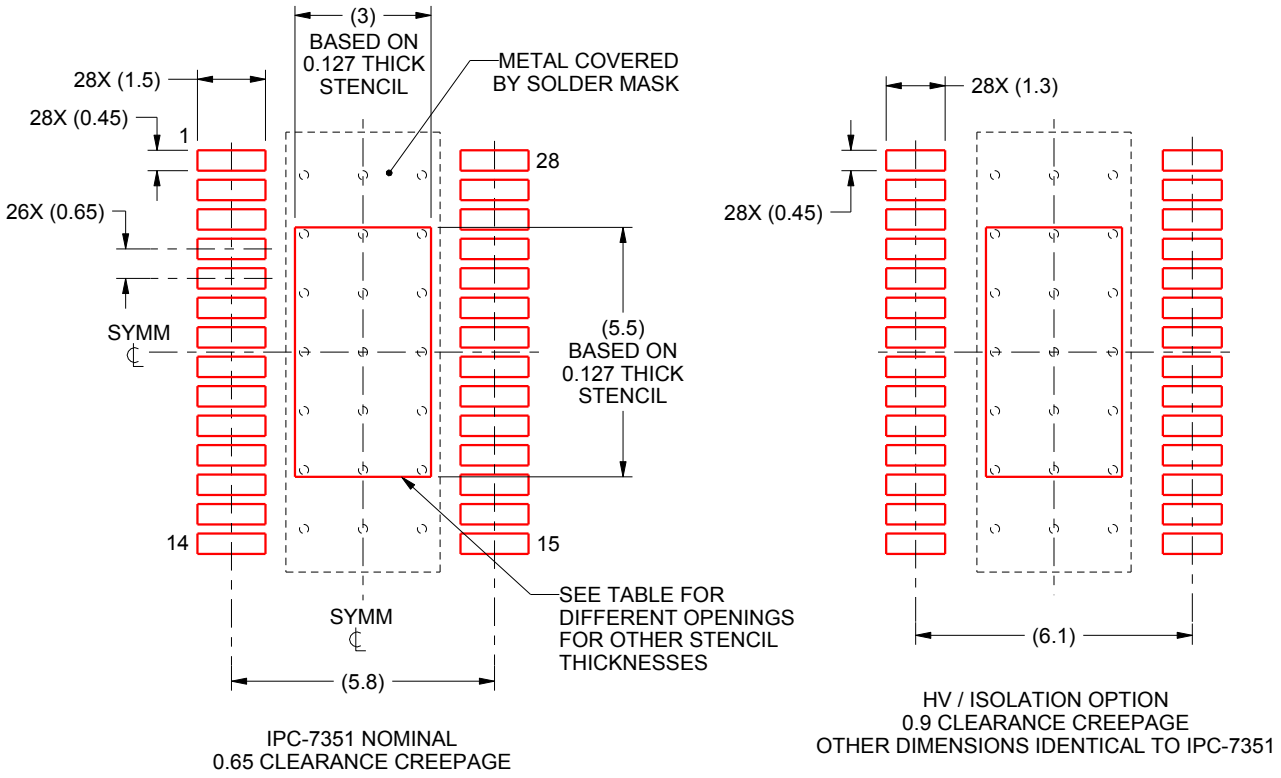
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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