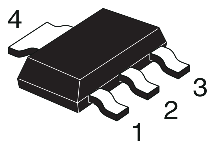
STN1NF20

N-channel 200 V, 1.1 Ω, 1 A SOT-223 STripFET™ II Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STN1NF20	200 V	< 1.5 Ω	1 A

- 100% avalanche tested
- Low gate charge
- Exceptional dv/dt capability



Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Figure 1. Internal schematic diagram

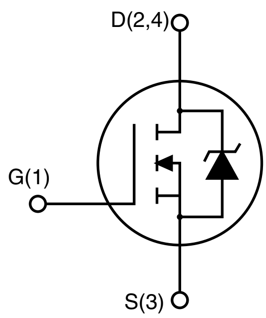


Table 1. Device summary

Order code	Marking	Package	Packaging
STN1NF20	1NF20	SOT-223	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current continuous T_{amb} = 25 °C	1	A
I_D	Drain current continuous T_{amb} = 100 °C	1	A
I_{DM} (1)	Drain current pulsed	4	A
P_{TOT}	Total dissipation at T_{amb} = 25 °C	2	W
dv/dt (2)	Peak diode recovery voltage slope	10	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. Isd ≤1 A, di/dt ≤200 A/µs, V_{DD} ≤80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction to ambient	62.50	°C/W

Table 4. Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive(1)	1	A
E_{AS}	Single pulse avalanche energy (2)	70	mJ

1. Pulse width limited by T_{JMAX}.
2. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 200 V V_{DS} = 200 V, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V, V_{DS}=0			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{GS} = V_{DS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.5 A		1.1	1.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	90 30 4	-	pF pF pF
R_g	Instrinsic gate resistance	f=1 MHz open drain	-	4.8	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 160 V, I_D = 1 A, V_{GS} = 10 V (see *Figure 14*)	-	5.7 1.1 3.0	-	nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$ t_r t_f $t_{c(off)}$	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 100 V, I_D = 0.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13*)	-	4 5.6 12.4 15.8	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		1 4	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 1 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1 A, di/dt = 100 A/µs V_{DD} = 20 V (see *Figure 15*)	-	51.8 90.7 3.5		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1 A, di/dt = 100 A/µs V_{DD} = 20 V, T_j = 150 °C (see *Figure 15*)	-	58.0 106.7 3.7		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

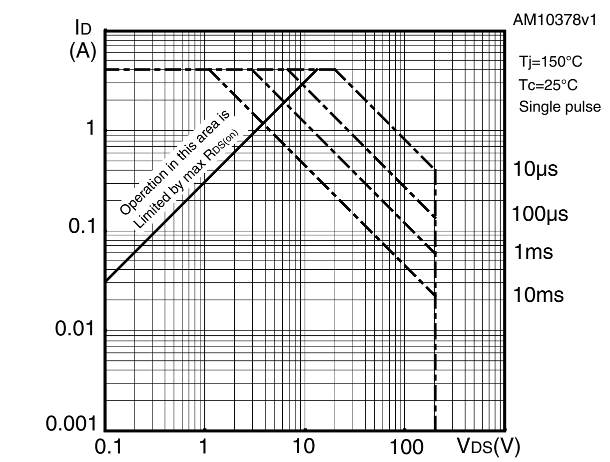


Figure 3. Thermal impedance

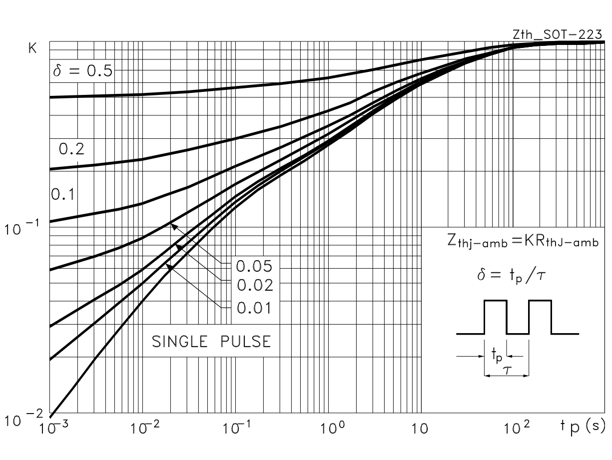


Figure 4. Output characteristics

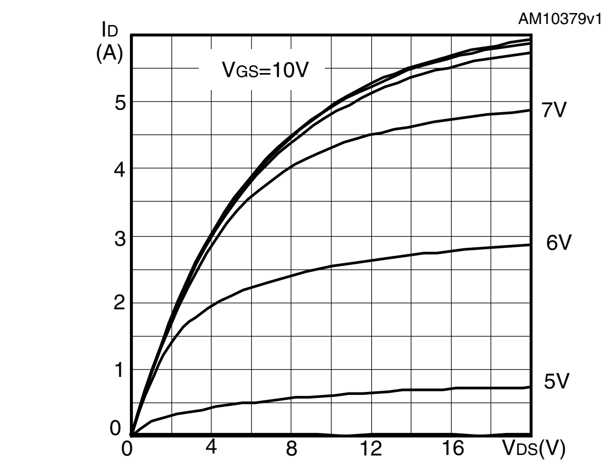


Figure 5. Transfer characteristics

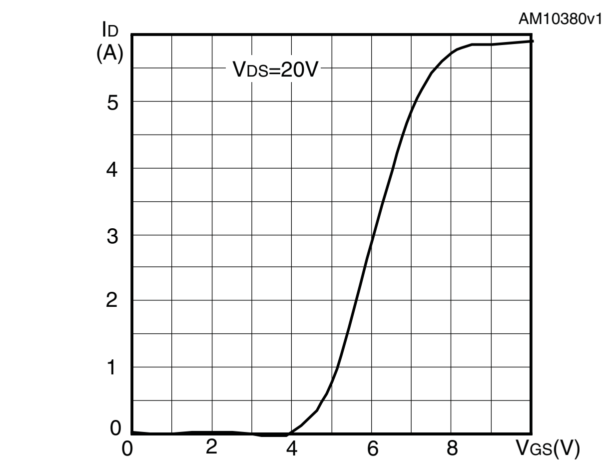


Figure 6. Normalized B_{VDSS} vs temperature

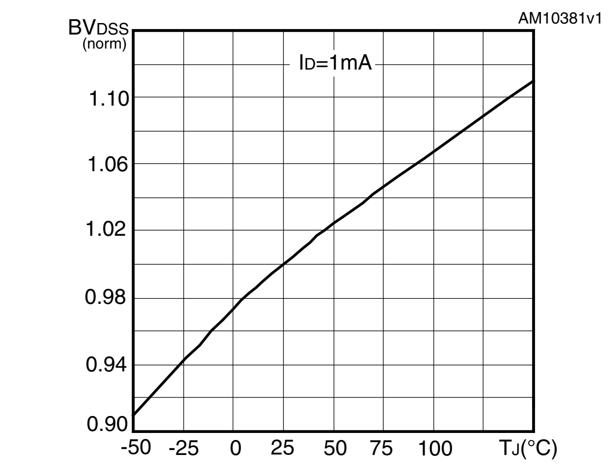


Figure 7. Static drain-source on resistance

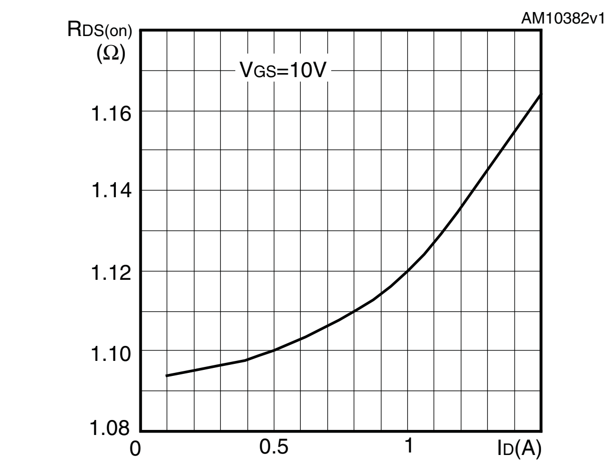


Figure 8. Gate charge vs gate-source voltage

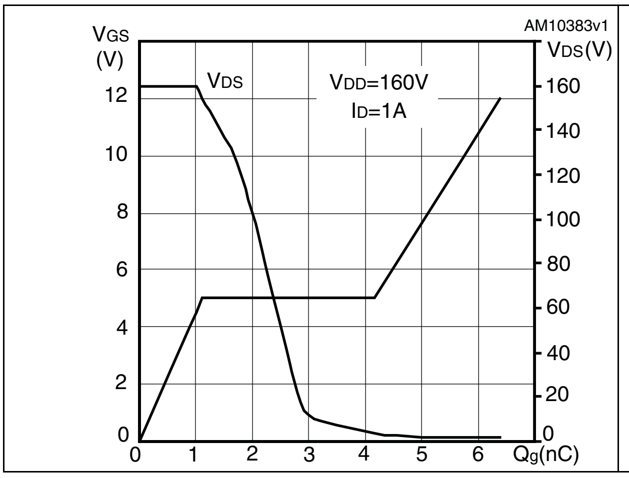


Figure 9. Capacitance variations

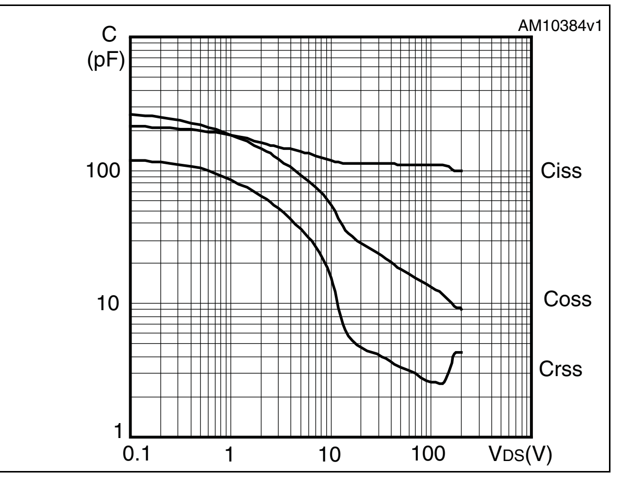


Figure 10. Normalized gate threshold voltage vs temperature

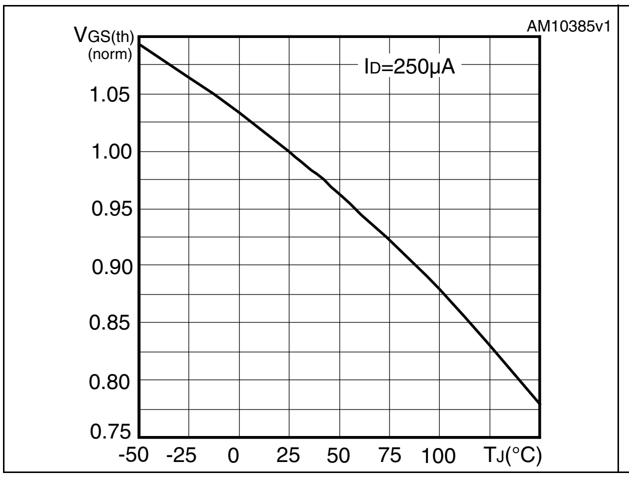


Figure 11. Normalized on resistance vs temperature

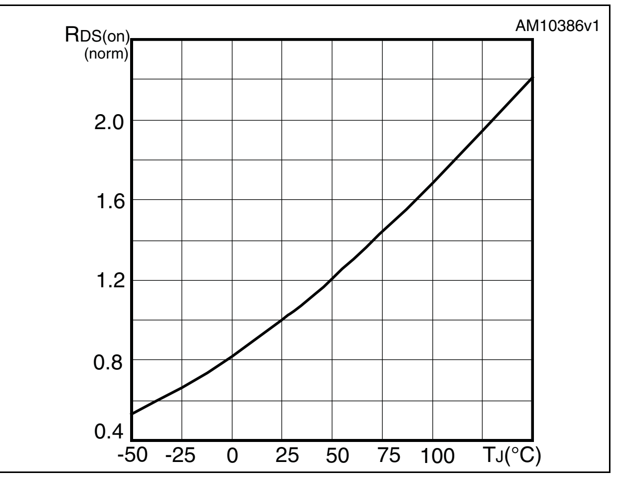
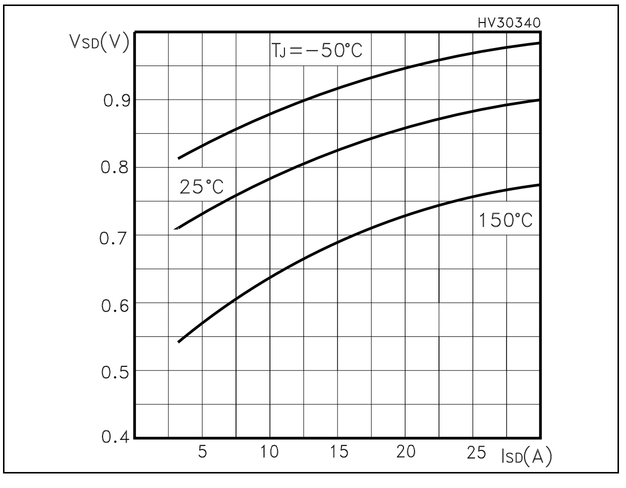


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

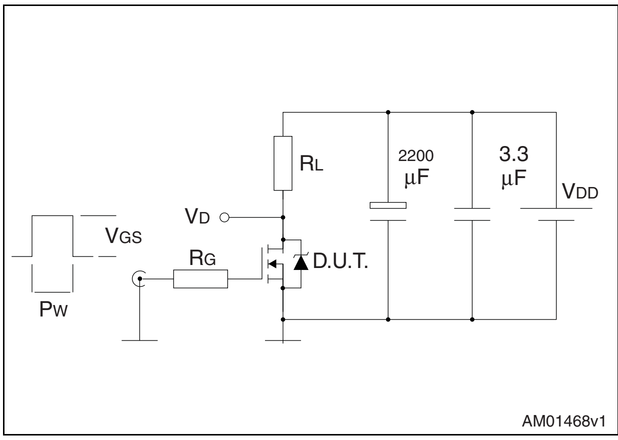


Figure 14. Gate charge test circuit

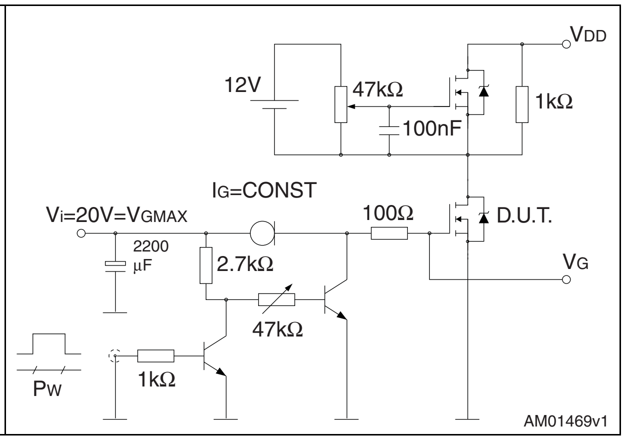


Figure 15. Test circuit for inductive load switching and diode recovery times

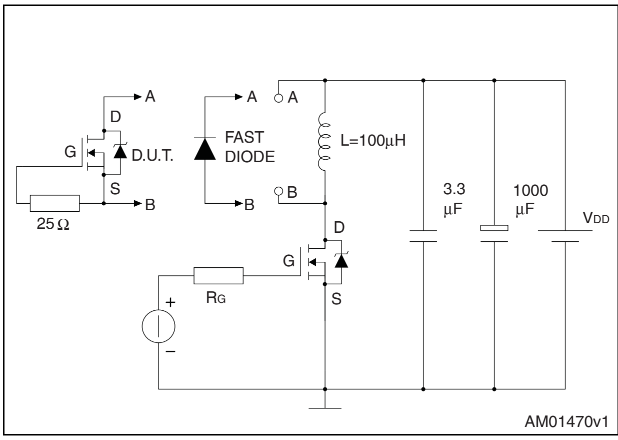


Figure 16. Unclamped inductive load test circuit

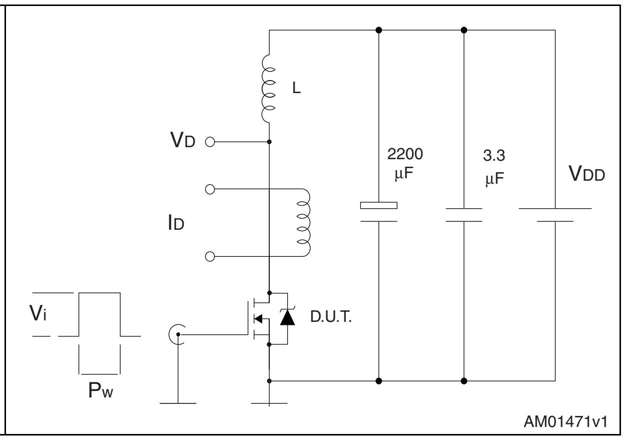


Figure 17. Unclamped inductive waveform

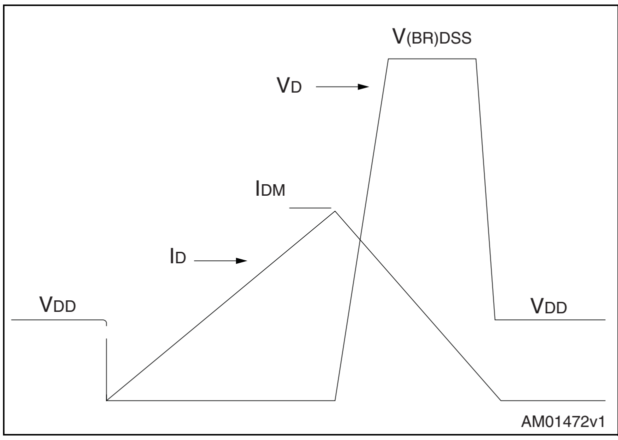
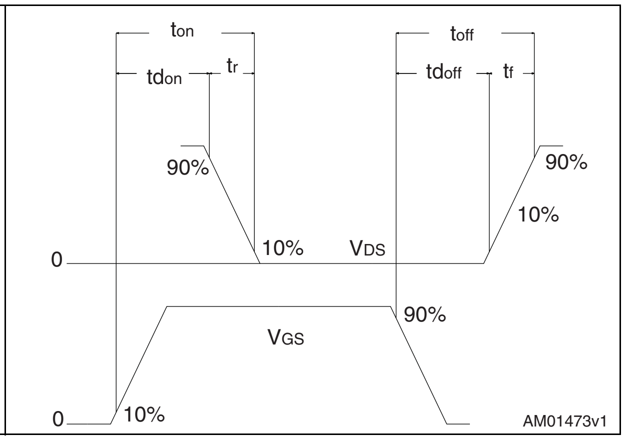


Figure 18. Switching time waveform



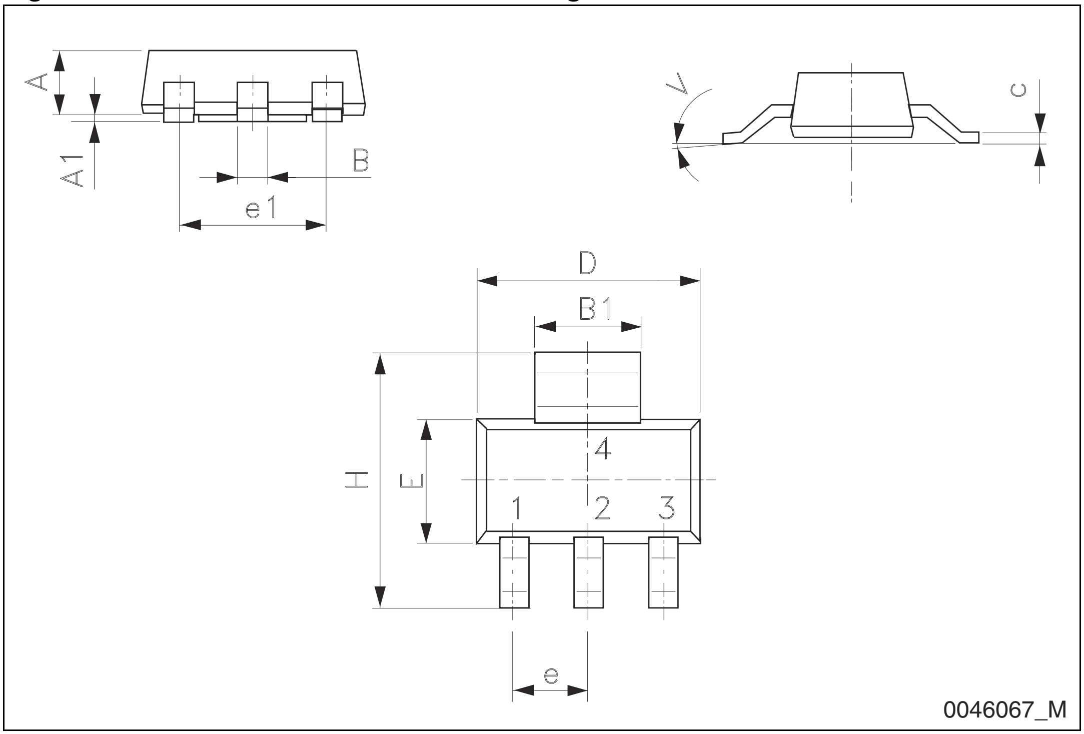
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10°

Figure 19. SOT-223 mechanical data drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
04-Nov-2011	1	First release.