74ABT652A

Octal transceiver/register; non-inverting; 3-state

Rev. 02 — 12 March 2010

Product data sheet

1. General description

The 74ABT652A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT652A transceiver/register consists of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin (CPAB or CPBA) goes HIGH. Output Enable (OEAB, OEBA) and Select (SAB, SBA) pins are provided for bus management.

2. Features and benefits

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-state outputs
- Live insertion/extraction permitted
- Power-up 3-state
- Power-up reset
- Output capability: +64 mA to –32 mA
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Ordering information

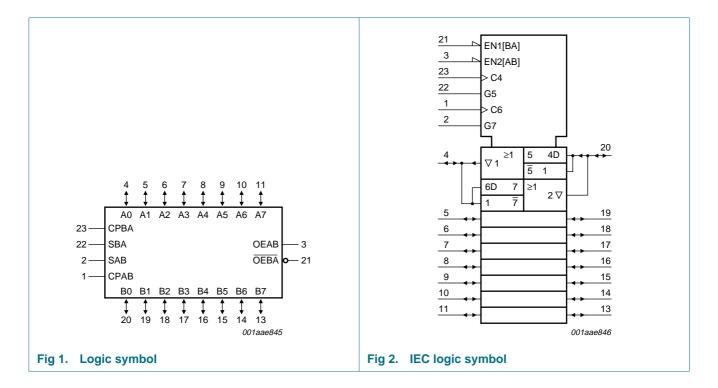
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT652AD	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT652ADB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT652APW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1



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4. Block diagram



Semiconductors

Octal transceiver/register; non-inverting; 3-state

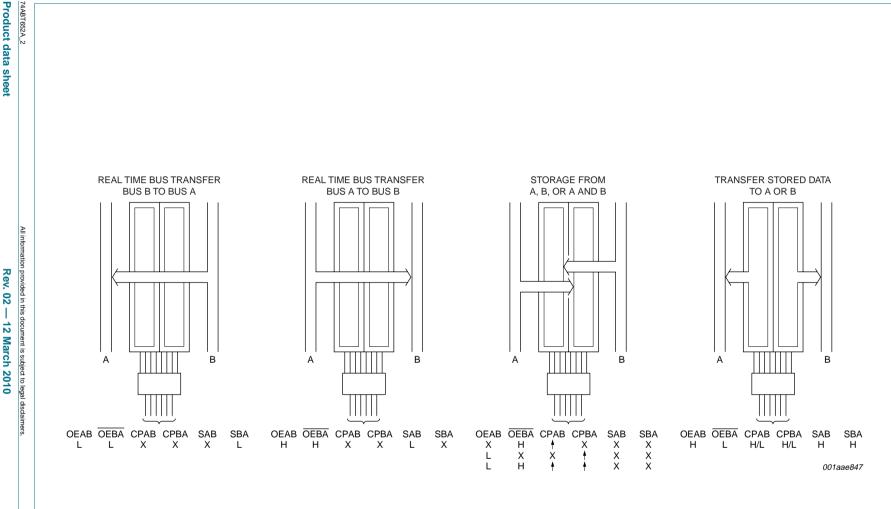
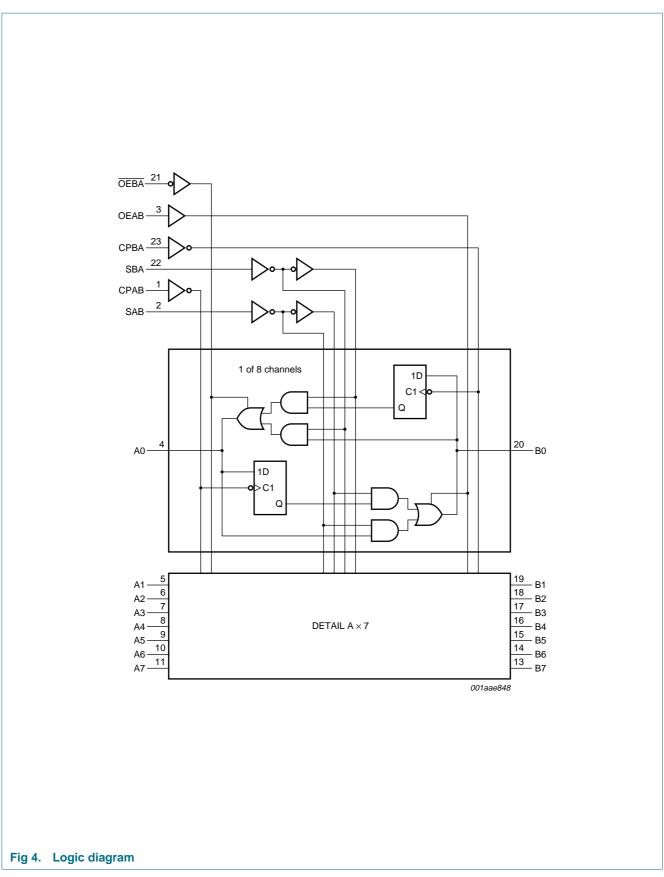


Fig 3. Real time bus transfer and storage

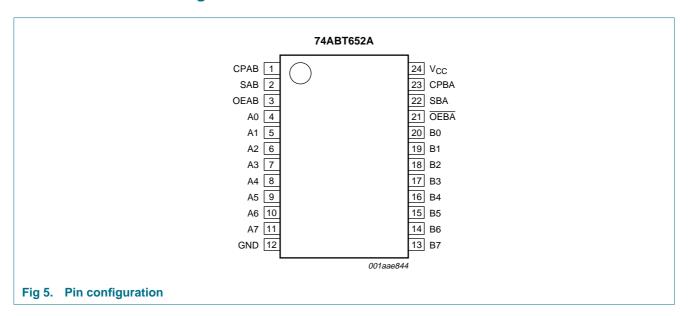
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Octal transceiver/register; non-inverting; 3-state

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Symbol	FIII	Description
CPAB	1	A to B clock input
SAB	2	A to B select input
OEAB	3	A to B output enable input
A0, A1, A2, A3, A4, A5, A6, A7	4, 5, 6, 7, 8, 9, 10, 11	data input/output (A side)
GND	12	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	20, 19, 18, 17, 16, 15, 14, 13	data input/output (B side)
OEBA	21	B to A output enable input (active LOW)
SBA	22	B to A select input
СРВА	23	B to A clock input
V _{CC}	24	positive supply voltage

Octal transceiver/register; non-inverting; 3-state

6. Functional description

6.1 Function table

Table 3. Function table [1]

Inputs						Data I/O		Operating mode
OEAB	OEBA	СРАВ	СРВА	SAB	SBA	An	Bn	
L	Н	H or L	H or L	X	Х	input	input	isolation
L	Н	1	1	Χ	Χ	input	input	store A and B data
X	Н	↑	H or L	X	Χ	input	unspecified output [2]	store A, hold B
Н	Н	↑	↑	[3]	Х	input	unspecified output [2]	store A in both registers
L	X	H or L	↑	X	Χ	unspecified output [2]	input	hold A, store B
L	L	↑	1	X	<u>[3]</u>	unspecified output [2]	input	store B in both registers
L	L	Χ	Х	Χ	L	output	input	real time B data to A bus
L	L	Χ	H or L	Χ	Н	output	input	stored B data to A bus
Н	Н	Χ	Х	L	Х	input	output	real time A data to B bus
Н	Н	H or L	Χ	Н	X	input	output	store A data to B bus
Н	L	H or L	H or L	Н	Н	output	output	stored A data to B bus; stored B data to A bus

^[1] H = HIGH voltage level;

- [2] The data output function may be enabled or disabled by various signals at the OEBA and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.
- [3] If both select controls (SAB and SBA) are LOW, then clocks can occur simultaneously. If either select control is HIGH, the clocks must be staggered in order to load both registers.

<u>Figure 3</u> demonstrates the four fundamental bus-management functions that can be performed with the 74ABT652A.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

L = LOW voltage level;

X = don't care:

 $[\]uparrow$ = LOW-to-HIGH clock transition.

Octal transceiver/register; non-inverting; 3-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_{I}	input voltage		<u>[1]</u> –1.2	+7.0	V
V_{O}	output voltage	output in OFF-state or HIGH-state	<u>[1]</u> –0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
lo	output current	output in LOW-state	-	128	mA
Tj	junction temperature		[2] _	150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{I}	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	8.0	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C

^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

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9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions			25 °C		–40 °C 1	Unit	
				Min	Тур	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$		-1.2	-0.9	-	-1.2	-	V
V_{OH}	HIGH-level output	$V_I = V_{IL}$ or V_{IH}							
	voltage	$V_{CC} = 4.5 \text{ V}; I_{OH} = -3 \text{ mA}$		2.5	3.0	-	2.5	-	V
		$V_{CC} = 5.0 \text{ V}; I_{OH} = -3 \text{ mA}$		3.0	3.5	-	3.0	-	V
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -32 \text{ mA}$		2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_{I} = V_{IL} or V_{IH}		-	0.3	0.55	-	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 5.5 V; I_{O} = 1 mA; V_{I} = GND or V_{CC}	<u>[1]</u>	-	0.13	0.55	-	0.55	V
I _I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V							
		control pins		-	±0.01	±1.0	-	±1.0	μΑ
		data pins		-	±5	±100	-	±100	μΑ
l _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$		-	±5.0	±100	-	±100	μΑ
I _{O(pu/pd)}	power-up/power-down output current	V_{CC} = 2.1 V; V_{O} = 0.5 V; V_{I} = GND or V_{CC} ; OEAB, \overline{OEBA} don't care	[2]	-	±5.0	±50	-	±50	μΑ
l _{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
		V _O = 2.7 V		-	5.0	50	-	50	μΑ
		V _O = 0.5 V		-	-5.0	-50	-	-50	μΑ
I _{LO}	output leakage current	V_{CC} = 5.5 V; HIGH-state; V_O = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	-	50	μΑ
Io	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	[3][5]	-180	-65	-40	-180	-40	mΑ
I _{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	110	250	-	250	μΑ
		outputs LOW-state		-	20	30	-	30	mΑ
		outputs disabled		-	110	250	-	250	μΑ
Δl _{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[4]	-	0.3	1.5	-	1.5	mA
Cı	input capacitance	$V_I = 0 \text{ V or } V_{CC}$		-	4	-	-	-	pF
Co	output capacitance	outputs disabled; $V_O = 0 \text{ V}$ or V_{CC}		-	7	-	-	-	pF

^[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

^[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. For V_{CC} = 2.1 V to V_{CC} = 5 V \pm 10 %, a transition time of up to 100 μ s is permitted.

^[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

^[4] This is the increase in supply current for each input at 3.4 V.

^[5] This data sheet limit may vary among suppliers.

Octal transceiver/register; non-inverting; 3-state

10. Dynamic characteristics

Table 7. Dynamic characteristics *GND = 0 V; for test circuit, see Figure 12.*

Symbol	Parameter	Conditions	25 °C	; V _{CC} =	= 5.0 V	-40 °C to V _{CC} = 5.0	Unit	
			Min	Тур	Max	Min	Max	
f _{max}	maximum frequency	see Figure 6	125	300	-	125	-	MHz
t _{PLH}	LOW to HIGH	CPAB to Bn or CPBA to An; see Figure 6	2.2	3.7	5.1	2.2	5.6	ns
	propagation delay	An to Bn or Bn to An; see Figure 7	1.5	3.0	4.3	1.5	4.8	ns
		SAB to Bn or SBA to An; see Figure 8	1.5	3.5	5.1	1.5	6.5	ns
t _{PHL}	HIGH to LOW	CPAB to Bn or CPBA to An; see Figure 6	1.7	4.3	5.1	1.7	5.6	ns
	propagation delay	An to Bn or Bn to An; see Figure 7	1.5	3.6	4.6	1.5	5.4	ns
		SAB to Bn or SBA to An; see Figure 8	1.5	4.2	5.2 <mark>[1]</mark>	1.5	5.9	ns
t _{PZH}	OFF-state to HIGH	OEBA to An; see Figure 10	2	3.2	4.6	2	5.8	ns
	propagation delay	OEAB to Bn; see Figure 10	2	3.5	6.1	2	6.5	ns
t _{PZL}	OFF-state to LOW	OEBA to An; see Figure 11	3	4.5	6.8	3	8.5	ns
	propagation delay	OEAB to Bn; see Figure 11	3	4.7	6.5	3	7.4	ns
t _{PHZ}	HIGH to OFF-state	OEBA to An; see Figure 10	1.5	3.9	4.7 <mark>[1]</mark>	1.5	5.3 <mark>[1]</mark>	ns
	propagation delay	OEAB to Bn; see Figure 10	1.5	3.8	4.6 <mark>[1]</mark>	1.5	5.5	ns
t _{PLZ}	LOW to OFF-state	OEBA to An; see Figure 11	1.5	2.9	3.8	1.5	4.1	ns
	propagation delay	OEAB to Bn; see Figure 11	1.5	3.0	4.4	1.5	5.1	ns
t _{su(H)}	set-up time HIGH	An to CPAB, Bn to CPBA; see Figure 9	3.0	0.7	-	3.0	-	ns
t _{su(L)}	set-up time LOW	An to CPAB, Bn to CPBA; see Figure 9	3.0	0.7	-	3.0	-	ns
t _{h(H)}	hold time HIGH	An to CPAB, Bn to CPBA; see Figure 9	0.0	-0.5	-	0.0	-	ns
t _{h(L)}	hold time LOW	An to CPAB, Bn to CPBA; see Figure 9	0.0	-0.5	-	0.0	-	ns
t _{WH}	pulse width HIGH	CPAB, CPBA; see Figure 6	4.0	1.0	-	4.0	-	ns
t_{WL}	pulse width LOW	CPAB, CPBA; see Figure 6	4.0	1.0	-	4.0	-	ns

^[1] This data sheet limit may vary among suppliers.

Octal transceiver/register; non-inverting; 3-state

٧_M

t_{PHL}

001aae904

11. Waveforms

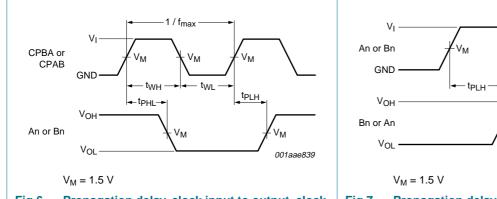
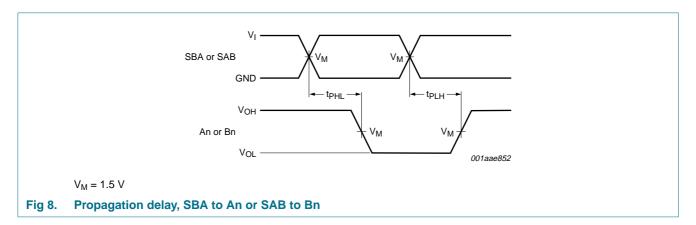
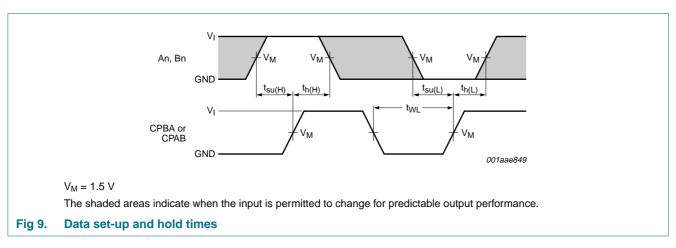


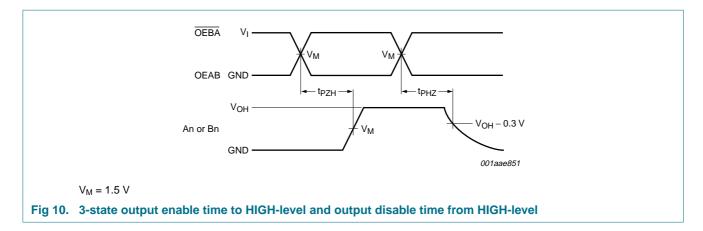
Fig 6. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency

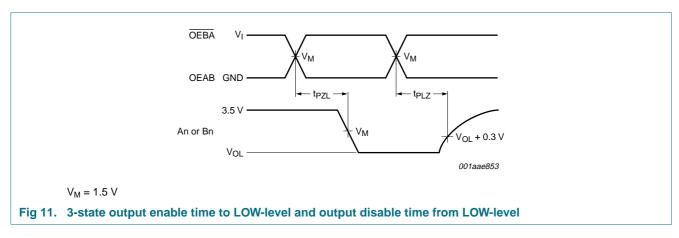




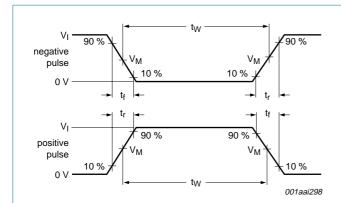


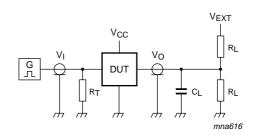
Octal transceiver/register; non-inverting; 3-state





Octal transceiver/register; non-inverting; 3-state





a. Input pulse definition

b. Test circuit

Test data and V_{EXT} levels are given in Table 8.

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{EXT} = Test voltage for switching times.

Fig 12. Test circuit for measuring switching times

Table 8. Test data

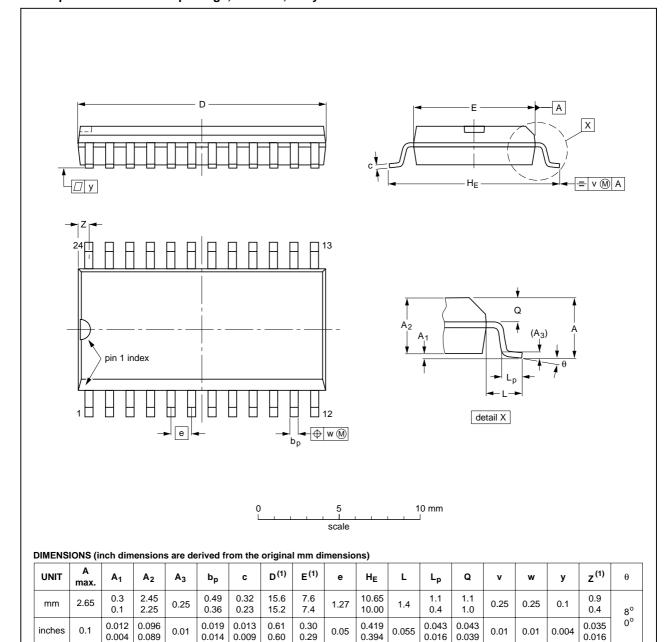
Input				Load		V _{EXT}			
VI	f_{l} t_{W} t_{r}, t_{f}		CL	C _L R _L		t _{PHL} , t _{PLH} t _{PZH} , t _{PHZ} t			
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500Ω	open	open	7.0 V	

Octal transceiver/register; non-inverting; 3-state

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT137-1	075E05	MS-013				-99-12-27 03-02-19

Fig 13. Package outline SOT137-1 (SO24)

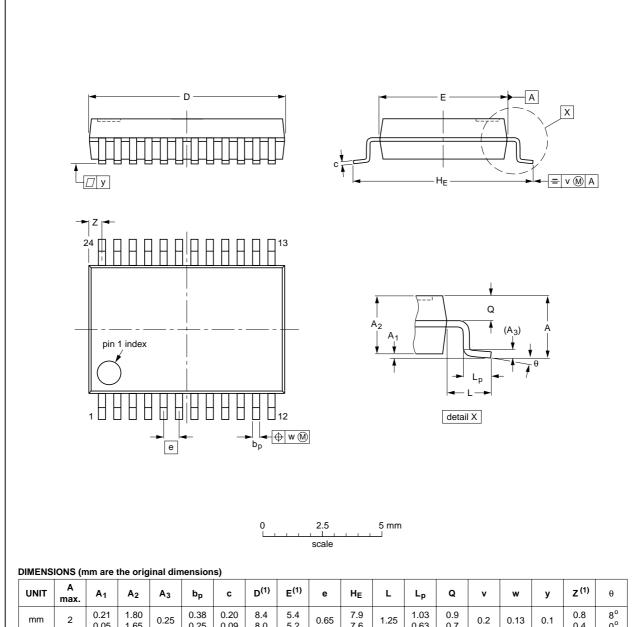
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Octal transceiver/register; non-inverting; 3-state

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE		REFER		EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT340-1		MO-150				99-12-27 03-02-19

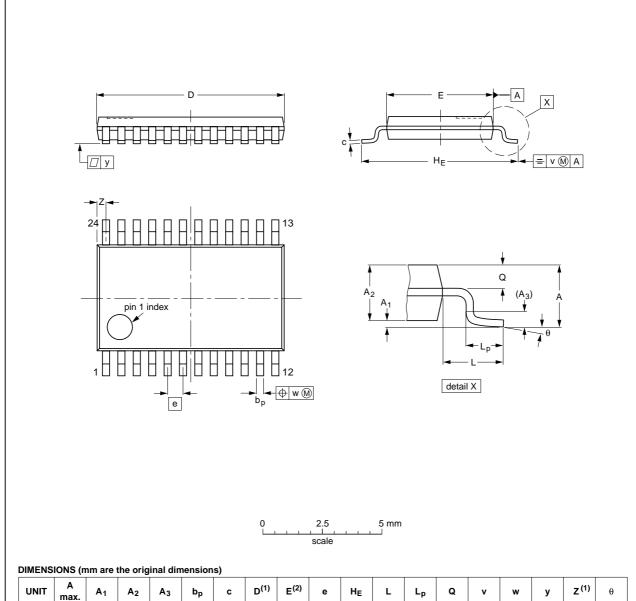
Fig 14. Package outline SOT340-1 (SSOP24)

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Octal transceiver/register; non-inverting; 3-state

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	U	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	ď	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN	ISSUE DATE		
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT355-1		MO-153				-99-12-27 03-02-19	

Fig 15. Package outline SOT355-1 (TSSOP24)

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Octal transceiver/register; non-inverting; 3-state

13. Abbreviations

Table 9. Abbreviations

Acronym	Description	
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
HBM	Human Body Model	
MM	Machine Model	

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74ABT652A_2	20100312	Product data sheet	-	74ABT652A		
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 					
	 Legal texts 	have been adapted to the r	new company name whe	ere appropriate.		
	• DIP 24 (SOT222-1) package removed from <u>Section 3 "Ordering information"</u> and <u>Section 12 "Package outline"</u> .					
74ABT652A	19950419	Product specification	-	-		

Octal transceiver/register; non-inverting; 3-state

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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