PCN Number:	20131122000	**PCN Date:**	12/02/2013
Title:	Qualification of Aizu and JCAP as additional Fab site and Assembly/Test site options for select devices in the CMOS9T 5V Fab process.		
Customer Contact:	PCN Manager	**Phone:**	+1(214)480-6037
Dept:	Quality Services		
***Proposed 1st Ship Date:**	03/02/2014	**Estimated Sample Availability:**	Date Provided at Sample request

Change Type:

☒	Assembly Site	☐	Assembly Process	☐	Assembly Materials
☐	Design	☐	Electrical Specification	☐	Mechanical Specification
☐	Test Site	☐	Packing/Shipping/Labeling	☐	Test Process
☐	Wafer Bump Site	☐	Wafer Bump Material	☐	Wafer Bump Process
☒	Wafer Fab Site	☐	Wafer Fab Materials	☐	Wafer Fab Process
		☐	Part number change		

PCN Details

Description of Change:

This change notification is to announce the addition of Aizu and JCAP as additional Fab site and Assembly/Test site options for select devices in the CMOS9T 5V Fab Process in Maine.

Group 1 (Fab Site):

Current Site/Process/Wafer Diameter	Additional Site/Process/Wafer Diameter
MAINEFAB/CMOS9T/200mm	AIZU/CMOS9T/200mm

Group 2 (Assembly Site):

TIEM	Assembly Site Origin (22L)	ASO: CU6
JCAP	Assembly Site Origin (22L)	ASO: JCP

The CMOS9T process was qualified at Aizu on 7/9/2013 and JCAP on 8/23/2013. Qualification results are shown below. Test coverage, insertions, conditions will remain consistent with current testing and verified with test MQ.

Reason for Change:

Continuity of supply.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Changes to product identification resulting from this PCN:

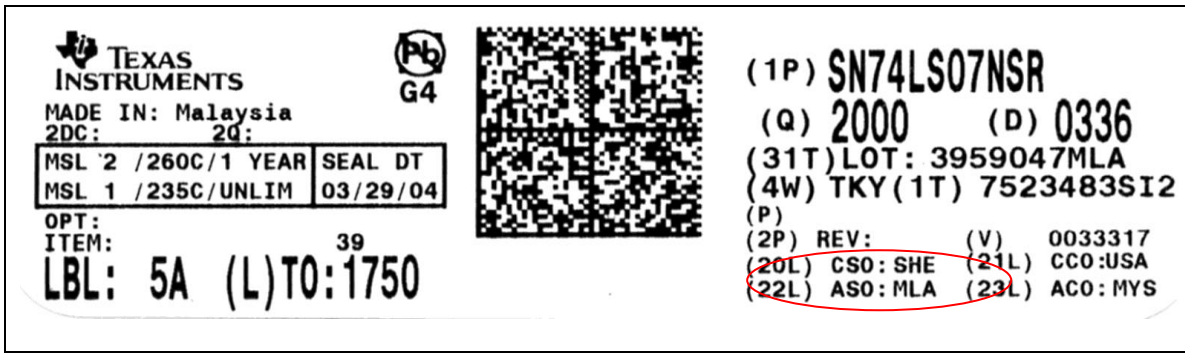
Sample Product Shipping Label (not actual product label)

Group 1:

Chip Site	Chip Site Code (20L)	Chip Country Code (21 L)
MAINEFAB	CUA	USA
AIZU	CU2	JPN

Group 2:

TIEM	Assembly Site Origin (22L)	ASO: CU6
JCAP	Assembly Site Origin (22L)	ASO: JCP



Product Affected Group 1 (Fab Site):			
LP8556TME-E01/NOPB	LP8556TME-E11/NOPB	LP8556TMX-E07/NOPB	LP8557E00AYFQT
LP8556TME-E02/NOPB	LP8556TME-E13/NOPB	LP8556TMX-E10/NOPB	LP8557IAYFQR
LP8556TME-E03/NOPB	LP8556TMX-E01/NOPB	LP8556TMX-E11/NOPB	LP8557IAYFQT
LP8556TME-E04/NOPB	LP8556TMX-E02/NOPB	LP8556TMX-E13/NOPB	LP8558AYFQR
LP8556TME-E05/NOPB	LP8556TMX-E03/NOPB	LP8557AYFQR	LP8558AYFQT
LP8556TME-E06/NOPB	LP8556TMX-E04/NOPB	LP8557AYFQT	LP8558E0AYFQR
LP8556TME-E07/NOPB	LP8556TMX-E05/NOPB	LP8557E00AYFQR	LP8558E0AYFQT
LP8556TME-E10/NOPB	LP8556TMX-E06/NOPB		

Product Affected Group 2 (Assembly Site):			
LP8556TME-E01/NOPB	LP8556TME-E11/NOPB	LP8556TMX-E07/NOPB	LP8557E00AYFQT
LP8556TME-E02/NOPB	LP8556TME-E13/NOPB	LP8556TMX-E10/NOPB	LP8557IAYFQR
LP8556TME-E03/NOPB	LP8556TMX-E01/NOPB	LP8556TMX-E11/NOPB	LP8557IAYFQT
LP8556TME-E04/NOPB	LP8556TMX-E02/NOPB	LP8556TMX-E13/NOPB	LP8558AYFQR
LP8556TME-E05/NOPB	LP8556TMX-E03/NOPB	LP8557AYFQR	LP8558AYFQT
LP8556TME-E06/NOPB	LP8556TMX-E04/NOPB	LP8557AYFQT	LP8558E0AYFQR
LP8556TME-E07/NOPB	LP8556TMX-E05/NOPB	LP8557E00AYFQR	LP8558E0AYFQT
LP8556TME-E10/NOPB	LP8556TMX-E06/NOPB		

Reference Qualification Data: CMOS9T Process at AIZU

Qualification Data: (Approved: 7/9/2013)			
This qualification has been developed for the validation of this change. The qualification data will validate that the proposed change meets the applicable released technical specifications.			
Qualification Device: LM5907UVX-3.3 (MSL LEVEL1-260C)			
Package / Die Attributes			
Wafer Fab Site:	AIZU	Assembly Site:	TIEM
Wafer Fab Process:	CMOS9T	# Pins-Designator:	4-YKE
Wafer Diameter:	200mm	Package Family:	YKE
Metallization:	AI .5%Cu	Bump Composition:	SnAgCu
Passivation:	PECVDOX/NITRIDE	Bump Diameter:	.2mm

Qualification: ☐ **Plan** ☒ **Test Results**				
Reliability Test	Conditions	Sample Size / Fail Lot#1	Lot#2	Lot#3
High Temp Operating Life	125C (1000 Hrs)	77/0	77/0	77/0
Early Life Failure Rate	125C (48 Hrs)	1000/0	1000/0	1000/0
**High Temp Storage Bake	150C (1000 Hrs)	77/0	77/0	77/0
**Biased Temp Humidity	85C/85%RH (500 Hrs)	77/0	77/0	77/0
**Autoclave	121C (96 Hrs)	77/0	77/0	77/0
**Temp Cycle	-65/150C (500 Cycles)	77/0	77/0	77/0
ESD CDM	500V	3/0	3/0	3/0
ESD HBM	1500V	3/0	3/0	3/0
Latchup	(per JESD78)	6/0	6/0	6/0
**Preconditioning: MSL1@260C				

Reference Qualification Data: CMOS9T Process at AIZU/JCAP

Qualification Data: (Approved: 8/23/2013)			
This qualification has been developed for the validation of this change. The qualification data will validate that the proposed change meets the applicable released technical specifications.			
Qualification Device: LP5907UVX2.85 (MSL LEVEL1-260C)			
Package / Die Attributes			
Wafer Fab Site:	AIZU	Assembly Site:	JCAP
Wafer Fab Process:	CMOS9T	# Pins-Designator:	4-YKE
Wafer Diameter:	200mm	Package Family:	YKE
Metallization:	AI .5%Cu	Bump Composition:	SnAgCu
Passivation:	PECVDOX/NITRIDE	Bump Diameter:	.2mm

Qualification: ☐ **Plan** ☒ **Test Results**				
Reliability Test	Conditions	Sample Size / Fail Lot#1	Lot#2	Lot#3
**Biased HAST	130C/85%RH (96 Hrs)	77/0	77/0	77/0
**Temp Cycle	-65/125C (500 Cycles)	77/0	77/0	77/0

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	**E-Mail**
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
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