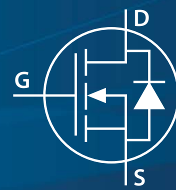
EPC2052 – Enhancement Mode Power Transistor

V_{DS} , 100 V
$R_{DS(on)}$, 13.5 mΩ
I_D , 8.2 A



EFFICIENT POWER CONVERSION

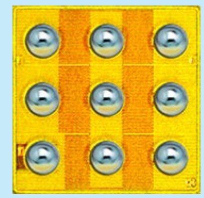
RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C)	8.2	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	74	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	2	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	15	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	74	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.



EPC2052 eGaN® FETs are supplied in passivated die form with solder bumps.
Die size: 1.5 mm x 1.5 mm

Applications

- 48 V Servers
- Lidar/Pulsed Power
- Isolated Power Supplies
- Point of Load Converters
- Class D Audio
- LED Lighting
- Low Inductance Motor Drive

Benefits

- Higher Switching Frequency – Lower switching losses and lower drive power
- Higher Efficiency – Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint - Higher power density

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.2 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 80 V, V_{GS} = 0 V, T_J = 25°C		0.02	0.15	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V, T_J = 25°C		0.01	1.8	mA
		V_{GS} = 5 V, T_J = 125°C		0.2	4	mA
	Gate-to-Source Reverse Leakage#	V_{GS} = -4 V, T_J = 25°C		0.01	0.18	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 3 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 11 A		10	13.5	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		2.0		V

Defined by design. Not subject to production test.

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V , V_{GS} = 0 V		441	584	pF
C_{RSS}	Reverse Transfer Capacitance			3.2		
C_{OSS}	Output Capacitance			195	293	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		227		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			274		
R_G	Gate Resistance			0.7		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 11 A		3.5	4.5	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 50 V, I_D = 11 A		1.5		
Q_{GD}	Gate to Drain Charge			0.5		
$Q_{G(TH)}$	Gate Charge at Threshold			1.0		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V		13	20	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

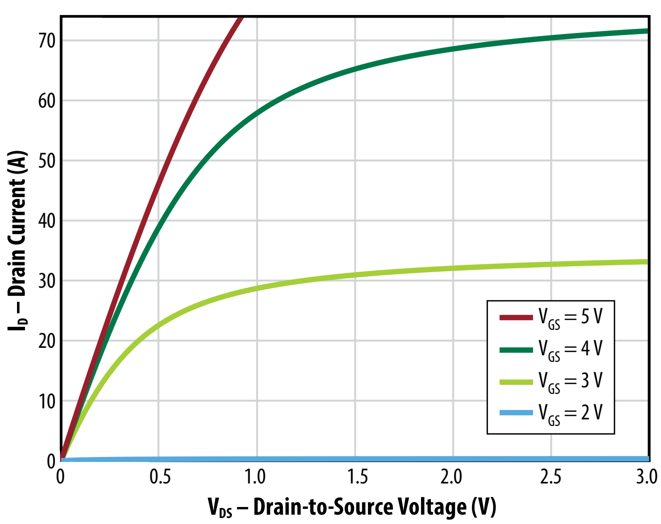


Figure 2: Typical Transfer Characteristics

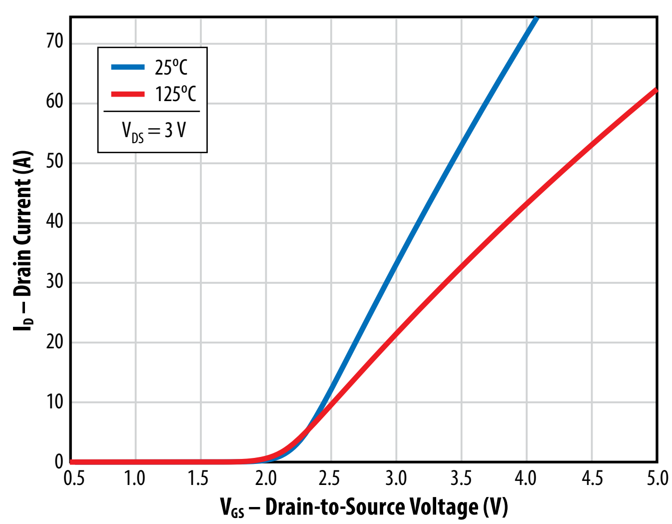


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Currents

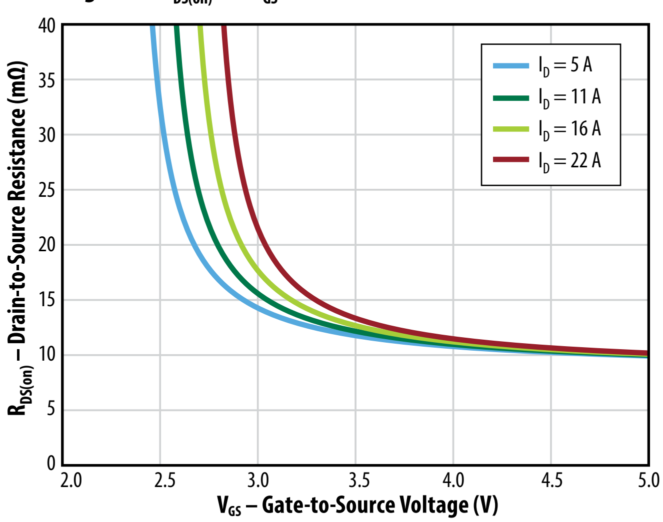
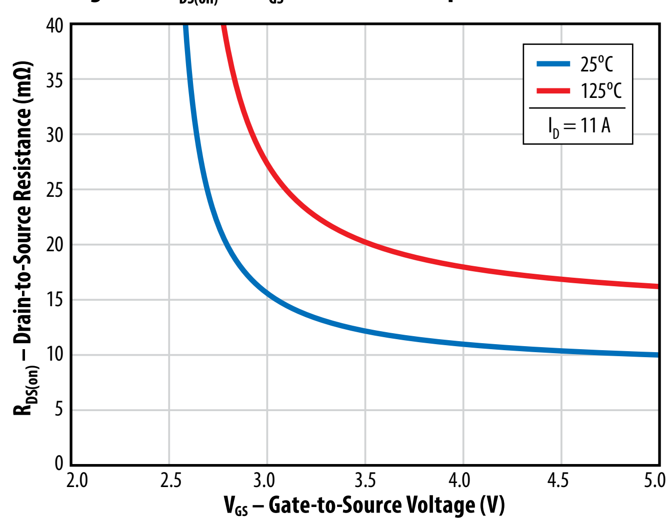


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures



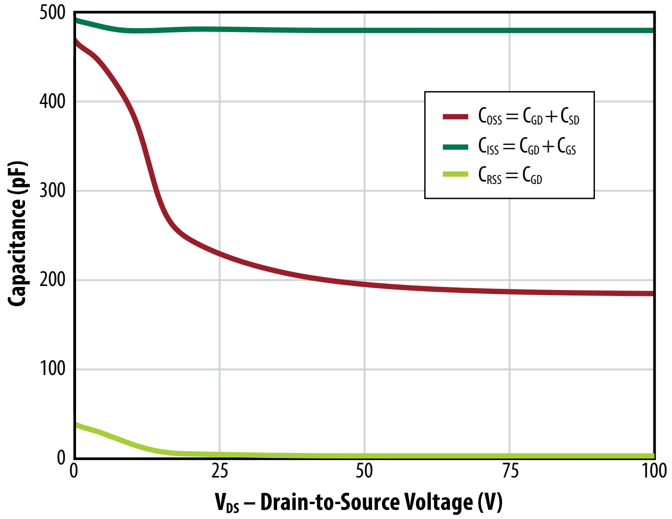


Figure 5a: Typical Capacitance (Linear Scale)

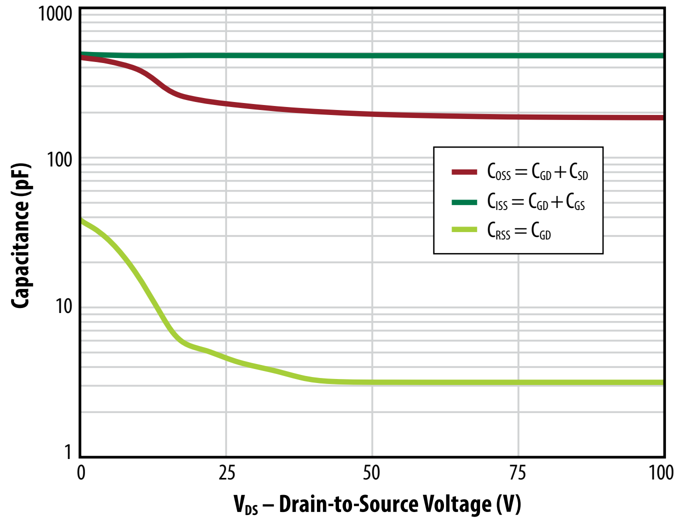


Figure 5b: Typical Capacitance (Log Scale)

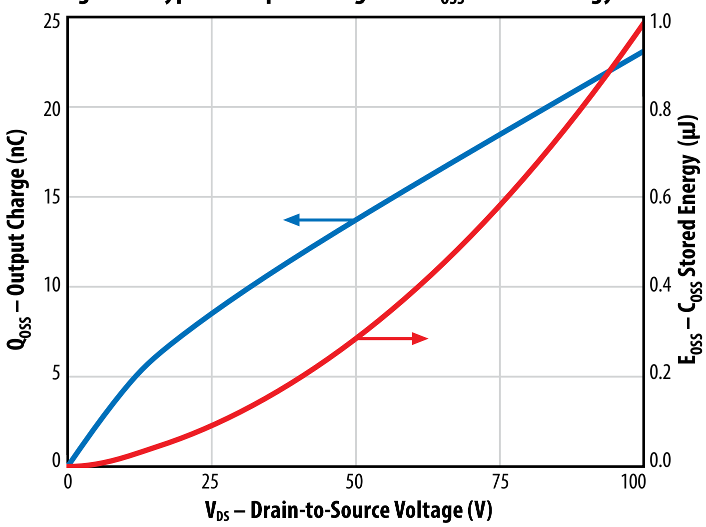


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

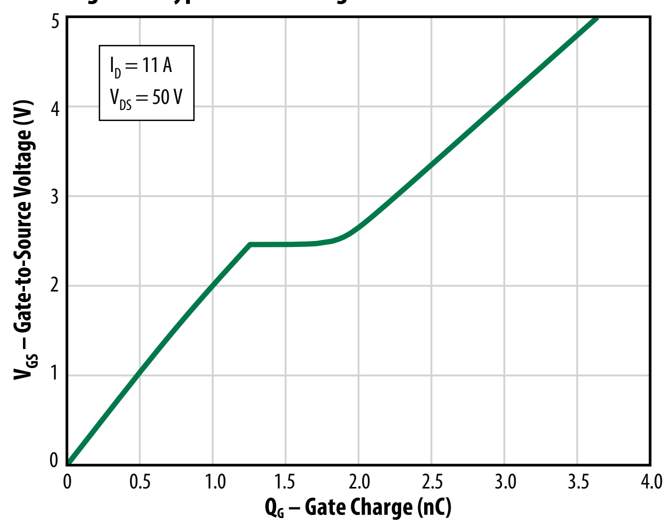


Figure 7: Typical Gate Charge

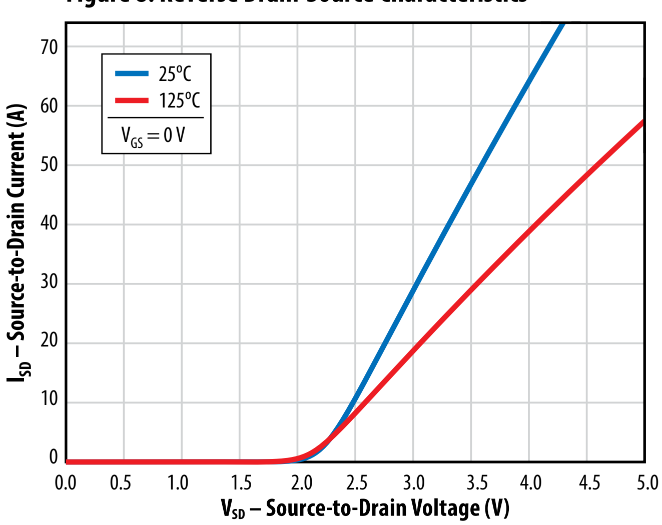


Figure 8: Reverse Drain-Source Characteristics

Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF

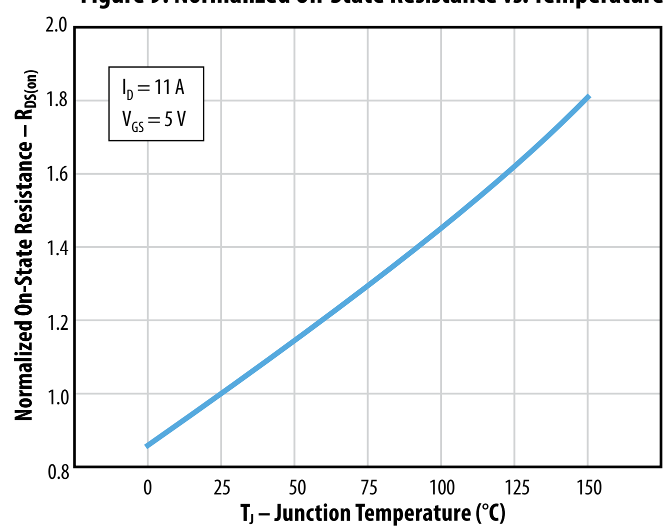


Figure 9: Normalized On-State Resistance vs. Temperature

Figure 10: Normalized Threshold Voltage vs. Temperature

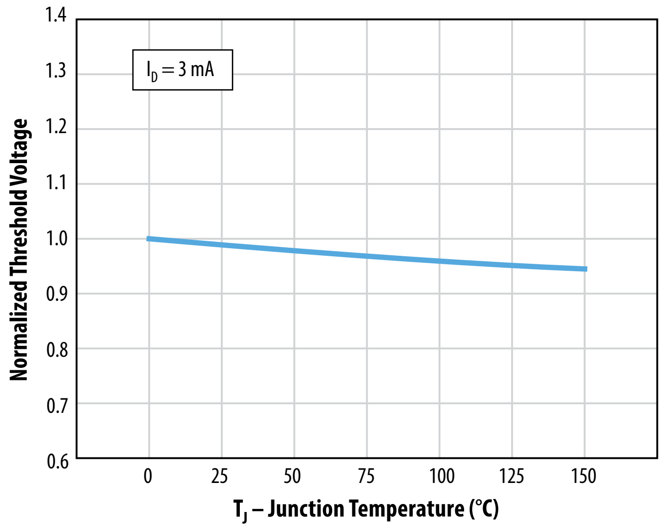
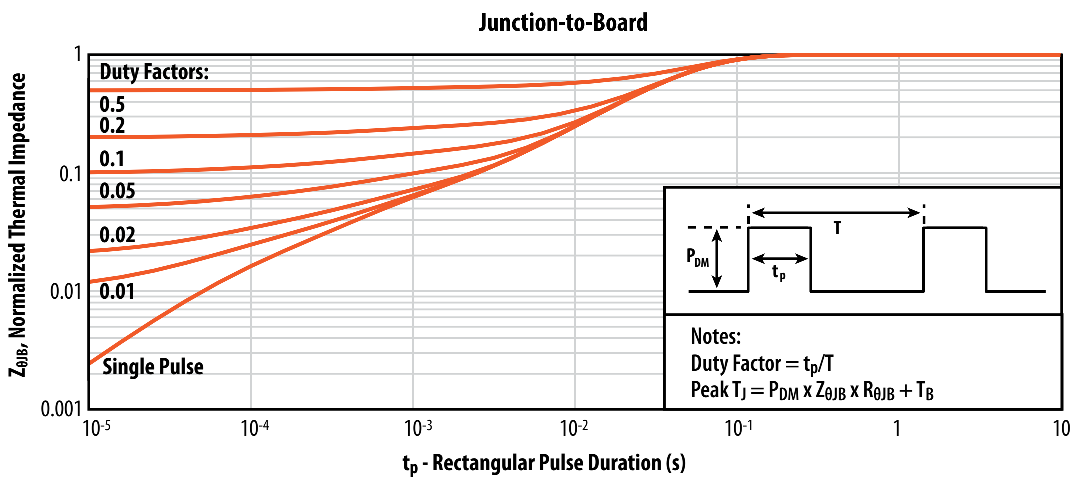


Figure 11: Transient Thermal Response Curves



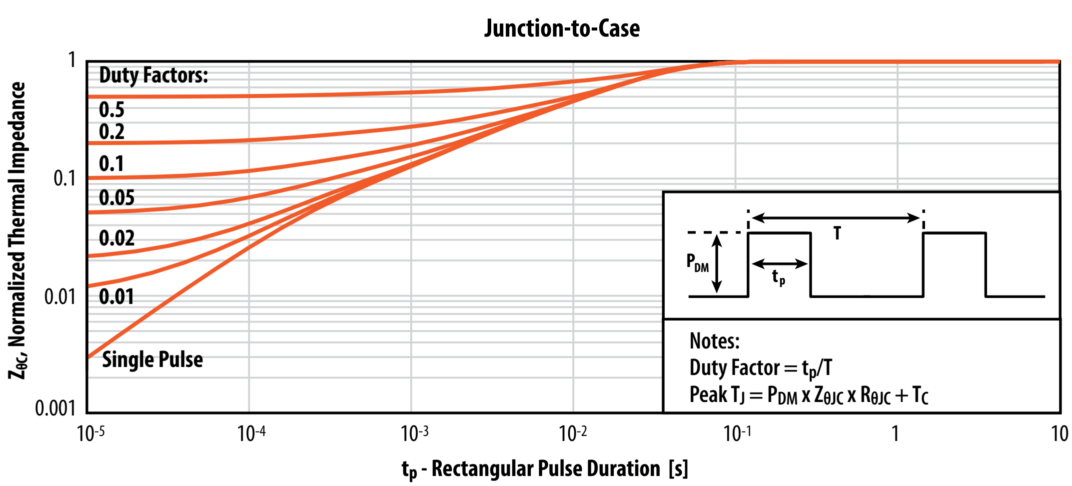
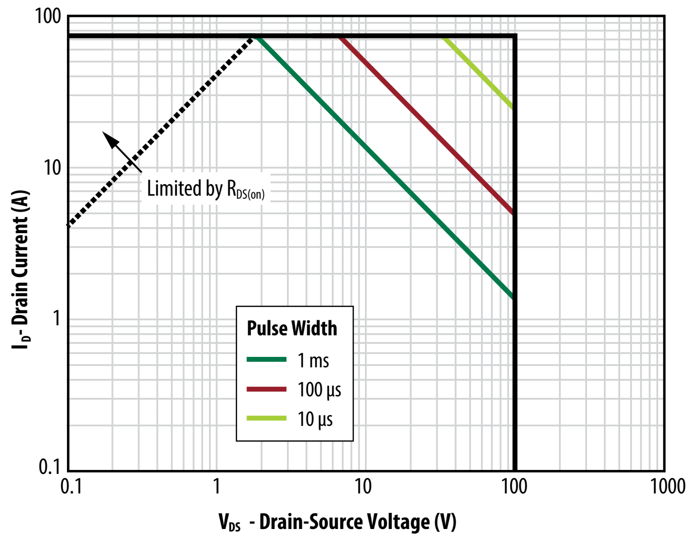


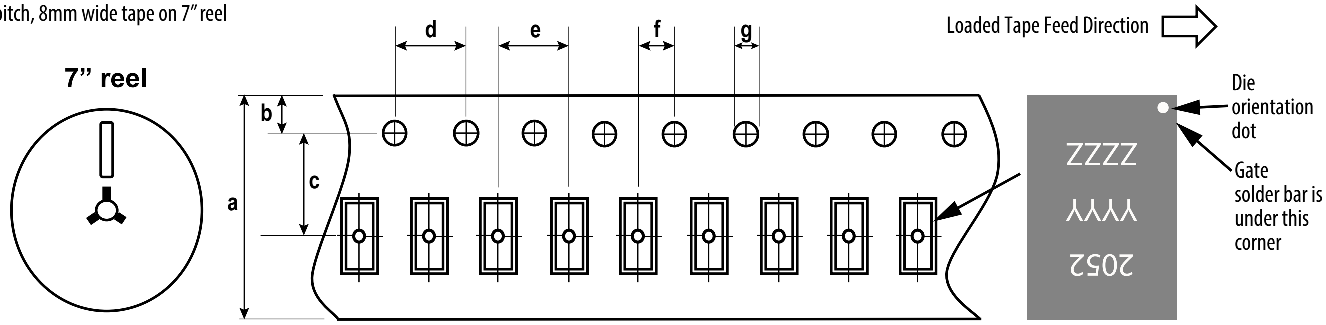
Figure 12: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

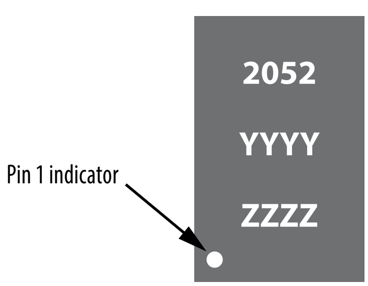


Die is placed into pocket solder bar side down (face side down)

Dimension (mm)	EPC2052 (note 1) target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS

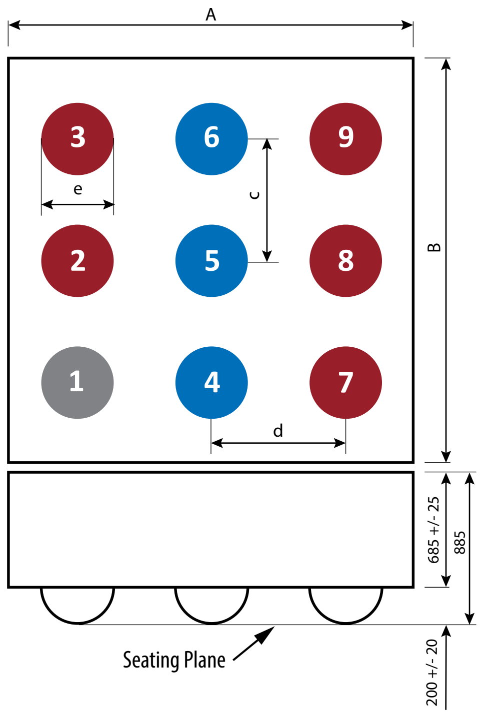


Part Number	Laser Markings Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2052	2052	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View

Side View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1470	1500	1530
B	1470	1500	1530
c		450	
d		500	
e	238	264	290

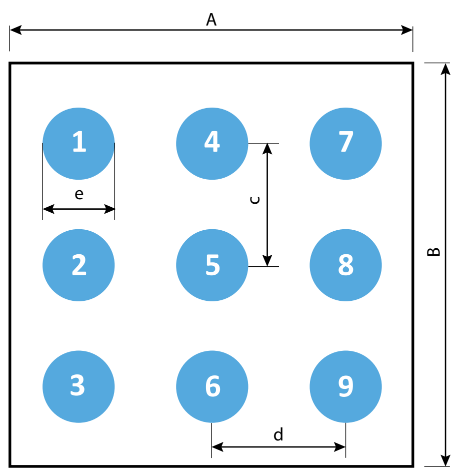
Pad 1 is Gate;

Pads 2, 3, 7, 8, 9 are Source;

Pads 4, 5, 6 are Drain.

RECOMMENDED LAND PATTERN

(units in µm)



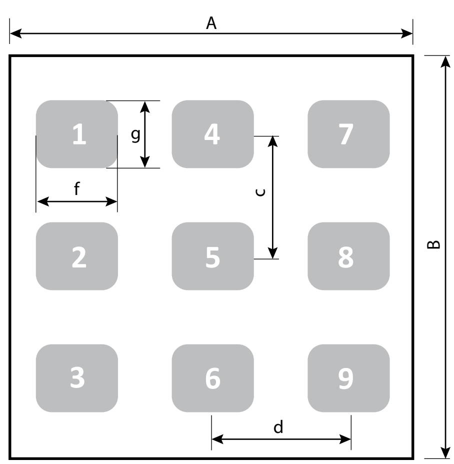
DIM	MICROMETERS
A	1500
B	1500
c	450
d	500
e	230

Pad 1 is Gate;
Pads 2, 3, 7, 8, 9 are Source;
Pads 4, 5, 6 are Drain.

RECOMMENDED STENCIL DRAWING

(measurements in µm)

Additional assembly resources available at https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx



DIM	MICROMETERS
A	1500
B	1500
c	450
d	500
f	300
g	250

Pad 1 is Gate;
Pads 2, 3, 7, 8, 9 are Source;
Pads 4, 5, 6 are Drain.

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, opening per drawing. The corner has a radius of R60. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Information subject to change without notice.
Revised September, 2022