

AM57xx Schematic Checklist

Catalog Processors

ABSTRACT

This application report points to examples and documents that specifically reference AM572x devices. They are equally applicable to AM571x devices, AM570x devices and AM574x devices. Links for additional AM57xx product pages and reference documents will be added as they become available.

Contents

1	Introduction	1
2	Recommendations Specific to AM57xx	3
3	References	13

List of Tables

1	Required PMIC Solutions	3
2	Proper RTC Connections	12

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1 Introduction

This article applies to the following devices:

- [AM5726BABCX](#)
- [AM5726BABCXA](#)
- [AM5726BABCXAR](#)
- [AM5726BABCXEA](#)
- [AM5728BABCX](#)
- [AM5728BABCXA](#)
- [AM5728BABCXEA](#)
- [AM5716AABCD](#)
- [AM5716AABCDA](#)
- [AM5716AABCDEA](#)
- [AM5716AABCX](#)
- [AM5716AABCXA](#)
- [AM5716AABCXEA](#)
- [AM5716AABCXEQ1](#)
- [AM5716AABCXQ1](#)
- [AM5718AABCX](#)
- [AM5718AABCXA](#)
- [AM5718AABCXEA](#)
- [AM5718AABCXEQ1](#)

- [AM5718AABCXQ1](#)
- [AM5706BCBDD](#)
- [AM5706BCBDDA](#)
- [AM5706BCBDDEA](#)
- [AM5706BCBDJ](#)
- [AM5706BCBDJA](#)
- [AM5706BCBDJEA](#)
- [AM5708BCBDJ](#)
- [AM5708BCBDJA](#)
- [AM5708BCBDJAR](#)
- [AM5708BCBDJEA](#)
- [AM5708BCBDJEAR](#)
- [AM5708BCBDJR](#)
- [XAM5746ABZXEA](#)
- [XAM5748ABZXEA](#)
- [XAM5749ABZXEA](#)

Throughout this document, the AM57xx device-specific Data Manual is referenced. Links to them are listed below for convenience:

- [AM5726](#)
- [AM5728](#)
- [AM5716](#)
- [AM5718](#)
- [AM5706](#)
- [AM5708](#)
- [AM5746](#)
- [AM5748](#)
- [AM5749](#)

Here are some links to some TI hardware designs based on AM57xx:

- [AM572x General Purpose EVM](#)
- [AM572x Industrial Development Kit EVM](#)
- [AM571x Industrial Development Kit EVM](#)
- [DRA71x/AM570x EVM](#)
- [AM570x 6-Layer PCB Reference Design](#)
- [AM574x Industrial Development Kit EVM](#)

Do not forget to check the device-specific Sitara™ Processors Silicon Errata document when designing a board. This document contains important information on silicon issues that will affect your board design.

- [AM572x Sitara™ Processors Silicon Revision 2.0, 1.1 Silicon Errata](#)
- [AM571x \(SR 2.0, 1.0\) and AM570x \(SR 2.1, 2.0\) Sitara™ Processors Silicon Errata](#)
- [AM574x Sitara™ Processors Silicon Revision 1.0 Silicon Errata](#)

Also check these other useful links:

- [AM574x, AM572x, and AM571x Compatibility Guide](#)
- [High-Speed Interface Layout Guidelines](#)
- [AM57xx BGA PCB Design](#)
- [AM57xx PCB Escape Routing Guidelines](#) wiki
- [TI PinMux Tool](#) wiki

2 Recommendations Specific to AM57xx

2.1 EVM vs Data Manual

In case of any discrepancy between the TI EVMs and the device-specific data sheet, always follow the data sheet. Despite the designer's best efforts, the EVMs may contain errors that still function but are not completely aligned with the data sheet specification. Therefore, the EVM designs should not be considered as reference designs to be blindly reused.

2.2 Power

Table 1. Required PMIC Solutions

	AM572x and AM574x		AM571x		AM570x	
Supported PMIC	TPS6590378	TPS6590379	TPS659162	TPS6590379	LP87332D + LP873220	TPS659163
TI EVM	AM572x EVM	AM572x IDK AM574x IDK	N/A	AM571x IDK	DRA71x/AM570x EVM	AM570x 6-layer Reference Design
PMIC User's Guide	TPS659037 User's Guide ⁽¹⁾	TPS659037 User's Guide ⁽¹⁾	TPS65916 User's Guide ⁽²⁾	TPS659037 User's Guide ⁽¹⁾	LP87332D and LP873220 User's Guide to Power AM570x ⁽³⁾	TPS65916 User's Guide to Power AM570x ⁽⁴⁾

(1) [TPS659037 User's Guide to Power AM574x, AM572x, and AM571x User's Guide](#)

(2) [TPS65916 User's Guide to Power AM571x User's Guide](#)

(3) [LP87332D and LP873220 User's Guide to Power AM570x User's Guide](#)

(4) [TPS65916 User's Guide to Power AM570x User's Guide](#)

- The AM57xx family of devices mandates the use of specific PMIC solutions. To see which PMIC needs to be used, see the device-specific data manual. You can also use [Table 1](#) for a summary of the specific AM57xx device to PMIC part mapping.
- Verify that the correct voltages are applied to the correct power pins on the chip and that the required current can be supplied.
- Zero Ω resistors in line with core and other power sections of the board are recommended for initial PCB prototype builds if you want to measure power consumption. Then, you should remove the resistor in production builds and connect the power planes with wide copper or multiple vias. Power measurement is the purpose of these resistors in the EVM designs. Note that the implementation of these resistors adds inductance and resistance that can impair power supply and power distribution performance.
- Proper power supply sequencing in proper correlation with resets and clocks is required. For the recommended power sequencing requirements, see the device-specific data manual.
- A TI SmartReflex™ solution is required for the VDD, VDD_MPU, VDD_GPU, VDD_IVA and VDD_DSPEVE rails of AM57xx devices. Using SmartReflex reduces device power consumption and ensures the proper operation across the temperature range. The AM57xx devices are used with PMIC power controllers such as those in the TPS659037x family that support the recommended SmartReflex implementation. Supported PMIC companion devices are referenced in the AM57xx device-specific data manual.
- Each of the VDDA_xxxxx power input pins should be connected to V1_8D through a filter circuit. In some cases, a single filter may be used for multiple pins.
- The DDR3 interface requires a VTT termination at the end of the flyby chain for the DDR3 address, command, control and clock signals. The VTT termination voltage is generated using a special push/pull termination regulator specifically designed to meet the VTT requirements for DDR3.
- The VTT regulator can provide the voltage rail for the DDR reference voltage, VREFSSTL also. If not, a voltage divider using tight tolerance (1% or better) resistors can also be used. If a resistor divider is used, the VREFSSTL source voltage MUST be generated from the VDDS_DDR supply so that it tracks that supply.

- AM57xx devices contain multiple analog power pins that provide power to sensitive analog circuitry like PLLs, DLLs and SERDES buffers and terminations. These must be attached to filtered power sources. These filter solutions must match the recommendations in the [AM57xx Hardware Design Guide](#).
- The AM572x EVM is configured to power up after the power button is pressed. If you prefer the board to start as soon as power is applied, see the *Powering On EVM* section of the [AM572x General Purpose EVM Hardware User's Guide](#). Similar capability exists on the AM57xx IDK EVMs. For more information on this capability, see the device-specific IDK EVM User's Guides.
- The internal LDO regulators on the AM57xx device require external capacitors connected to their output pins (CAP_VBBLDO_MPU1, CAP_VDDRAM_DSPEVE1, CAP_VDDRAM_CORE2, and so forth). Be sure to place a 1 μ F capacitor from each of these LDO outputs to ground (VSS). For the list of LDO outputs, see the AM57xx device-specific data manual. These capacitors must be placed as close to the respective pin as possible (within 0.25" of the package boundary).
- Ensure current capabilities of DC/DC switchers and LDOs meet the maximum demand of all devices that are attached. You can find the maximum current draw of all AM57xx power rails by using the Power Estimation Tool available for your specific device. If the outputs from the PMIC also power other devices, the maximum current draw of these devices need to be taken into consideration as well.
- The PMIC will control the supply sequencing so that it meets the requirements of the AM57xx device during start-up. It will also properly control the sequencing during shut-down as long as it is properly powered during this period. A detect circuit such as a TPS3808 can monitor the main supply input and initiate the shut-down sequence when the main supply starts to drop by driving the RESET_IN to the PMIC. Sufficient capacitance is required to hold up the main supply to the PMIC for at least 1.1 ms after RESET_IN is driven low for the sequence to complete.
- Ensure I2C1 is used for communication to PMIC. All TI software distributions assume the use of this interface with the PMIC.
- The LVCMOS Input/output pins powered from the VDDSHVxx supplies support both 3.3 V and 1.8 V nominal power supplies. During power-up, operation and power-down, the VDDSHVxx supplies set at 3.3 V nominal cannot be more than 2.0 V above the VDD18V supply voltage. This is shown in the AM57xx device-specific data manual. A voltage clamp circuit is needed to assure this restriction is met. An example of this circuit can be found in the *Use of a Clamping Circuit for Simultaneous Ramp Down* section of [Powering the AM335x With the TPS650250](#). This is not required for 3.3 V supplies derived from LDOs or SMPS9 of the TPS659037x PMIC. This circuit is required if using a 3.3 V supply enabled through a power switch that is controlled by REGEN1 unless you can prove that the shut-down sequence will be met.
- Be sure to use low ESL capacitors and mount them with short traces to keep the mounting inductance very low. This is required to meet the specified PDN impedance. For more information, see [Sitara™ Processor Power Distribution Networks: Implementation and Analysis](#).
- PMIC SMPS converters have "remote sense" or SMPSx_FDBK inputs. These must be connected at the load (or even the far side of the load), not at the PMIC output. The IR drop in the power distribution routing can result in the load not getting sufficient voltage. A 0- Ω resistor can be put at the end of each of these traces to enforce the routing to the proper sense point.
- To aid customers designing with the TPS659037x family of PMICs, see the [TPS659037 Design Guide](#).
- To aid customers designing with the TPS659037x family of PMICs, see the [TPS659037 Design Checklist](#).
- For detailed recommendations on connecting and routing, see the [TPS659037 User's Guide to Power AM574x, AM572x, and AM571x User's Guide](#).

NOTE: Be sure to connect a 2.2 μ F capacitor between the OSC16MCAP pin and ground as required when using the TPS659037x PMICs recommended for AM57xx devices.

2.3 Reset

- The hard reset PORZ is best if driven from power good circuitry to assure proper sequencing such that power is stable and input clock signals are stable before PORZ is released. For details about the requirements of PORZ, see the device-specific data manual.
- Reset pins must be driven as defined in the device-specific data manual. This sequencing in relation to clocks and power supply ramping must be followed in all operating conditions, including boundary scan testing.
- PORZ must be held low until all supplies have been stable for some time. Conversely, PORZ must be pulled low before any supply rails begin power down - especially in any unexpected power-loss situations.
- The PORZ pin has special properties such that it holds all output pins at high impedance when low. When controlled from logic derived from a power good indication, it can safely shut down the device and prevent output contention resulting in harmful current flow if a power supply fault occurs.
- All control pins must be held at the proper input level prior to the reset signal rising that releases the device from reset.
- RSTOUTn is driven low whenever the device enters the reset state. RSTOUTn is undefined during supply ramp. Ensure peripheral reset inputs can handle this. If glitches during power-up are a concern, peripheral resets generated from RSTOUTn can be AND'ed with PORz. This will block the possible glitches from propagating during supply ramp.
- There is an erratum that requires all reset events to trigger a PORz - i862 Reset Should Use PORz. This can be implemented through an external PORz pulse generator as shown on the GP EVM or implemented using a feature of the PMIC as shown on the IDK EVM. Both solutions are valid but result in design tradeoffs. This is documented in detail in the AM57xx device-specific errata document under i862.

NOTE: If you are using the PMIC feature to workaround errata i862, make sure you do not have a pullup on RSTOUTn as it will cause an infinite reboot loop.

2.4 Boot Modes

- SYSBOOT pins must be properly configured to set the proper boot mode at reset release. These can be set by resistor population or driven from logic such as an FPGA.
- SYSBOOT15
 - AM574x:
 - SYSBOOT15 is configurable. In short, it should be pulled high if booting from eMMC and pulled low for booting from parallel NOR flash. For complete details, see the *Permanent PU/PD Disabling* section in the [AM574x Sitara™ Processors Silicon Revision 1.0 Technical Reference Manual](#).
 - AM572x:
 - For Silicon Revision 1.x, SYSBOOT15 must be tied to VDD.
 - For Silicon Revision 2.0, SYSBOOT15 is configurable. In short, it should be pulled high if booting from eMMC and pulled low for booting from parallel NOR flash. For complete details, see the *Permanent PU/PD Disabling (SR 2.0 only)* section in the [AM572x Sitara™ Processors Silicon Revision 2.0, 1.1 Technical Reference Manual](#).
 - AM571x:
 - For Silicon Revision 1.0, SYSBOOT15 must be tied to VDD.
 - For Silicon Revision 2.0, SYSBOOT15 is configurable. In short, it should be pulled low if booting from eMMC and pulled high for booting from parallel NOR flash. For complete details, see the *Permanent PU/PD Disabling (SR 2.0 only)* section in the [AM571x \(SR2.0, SR1.0\) AM570x \(SR2.1, SR2.0\) Sitara™ Processors Technical Reference Manual](#).

- AM570x:
 - For Silicon Revision 2.1, SYSBOOT15 is configurable. In short, it should be pulled low if booting from eMMC and pulled high for booting from parallel NOR flash. For complete details, see the *Permanent PU/PD Disabling (SR 2.0 only)* section in the [AM571x \(SR2.0, SR1.0\) AM570x \(SR2.1, SR2.0\) Sitara™ Processors Technical Reference Manual](#).
 - If the SYSBOOT pins are redefined for another purpose during operation, they must be released and set back to the proper levels to select the boot mode whenever PORz goes low and they must remain unchanged for the defined hold duration after PORz rising per the device-specific data manual.
 - SYSBOOT14 must be tied to VSS.

2.5 Unused Signals

Signals on interfaces that are unused can typically be left as no connect. Many of the IOs have a Pad Configuration Register that provides control over the input capabilities of the I/O (INPUTENABLE field in each conf_<module>_<pin> register). For more information, see the *Control Module* chapter of the device-specific TRM. Software should disable the RX buffers that are no connects (INPUTENABLE=0) as soon as possible during initialization. This INPUTENABLE field defaults to "input active" for most signals, which means there is a potential for some leakage during powerup of the chip if the input floats to a mid-supply level before the software can initialize the I/O. This should only be a concern if you are attempting to power up the design with a minimum power consumption. Most designs should be able to tolerate this small amount of leakage in each floating I/O until the software has a chance to disable it. After disabling the receiver of the I/O, no leakage will occur.

NOTE: For specific guidance on certain unused pins, see the Unused Balls Connection Requirements section in the device-specific data manual.

2.6 Unused OSC1

If OSC1 is unused, be sure that the xi_osc1 pin is grounded or pulled low.

2.7 Unused Power Rails

This section provides guidance for power supply inputs when the associated interface is not used. Unless stated otherwise, a voltage at the rated level must still be provided. Also, this supply voltage must still ramp up and ramp down in accordance with the timing and sequence requirements stated in the device-specific data manual.

Unless stated explicitly below, filter elements and high frequency decoupling capacitors are not needed for the power supply inputs associated with unused interfaces. If a filter element is still required, a single 0.1 μ F capacitor at the supply pins will be sufficient to keep the voltage stable.

2.7.1 If DDR1 is not Used

- Connect the VDDS_DDR1 terminals to either 1.35 V or 1.5 V
- Connect the VDDS18V_DDR1 to 1.8 V
- Connect the DDR1_VREF0 to 0.5*VDDS_DDR1

2.7.2 If DDR2 is not Used

- Connect the VDDS_DDR2 terminals to either 1.35 V or 1.5 V
- Connect the VDDS18V_DDR2 to 1.8 V
- Connect the DDR2_VREF0 to 0.5*VDDS_DDR2

2.7.3 If USB1, USB2, or USB3 are not Used

- Connect the respective VDDA_USB1, VDDA_USB2, VDDA_USB3 terminal to 1.8 V - no filtering is needed when respective interface is unused
- VDDA33V_USB1/2
 - AM574x/AM572x/AM571x: Connect VDDA33V_USB1 or VDDA33V_USB2 terminal directly to any 3.3 V power supply. No decoupling is required in this case. If the system does not have a 3.3 V power supply, these terminals may be connected to ground.
 - AM570x: The VDDA33V_USB1 or VDDA33V_USB2 terminal must be connected to a 3.3 V power supply since this rail also powers digital IO buffers.

2.7.4 If HDMI is not Used

- VDDA_HDMI should be connected through a filter element to 1.8 V.

2.7.5 If PCIe is not Used

- VDDA_PCIE, VDDA_PCIE0, VDDA_PCIE1 should be connected to 1.8 V through a common filter element.

2.7.6 If SATA is not Used

- VDDA_SATA should be connected to 1.8 V through a filter element.

2.7.7 If RTC Internal Oscillator is not Used

This can be the case when either the internal system clock is used or a 1.8 V LVCMOS clock source is used rather than a crystal circuit or the RTC is not used at all. If a 1.8 V LVCMOS clock source is used then:

- Connect the clock source to the RTC_OSC_XI_CLKIN32 terminal
- Leave the RTC_OSC_XO terminal open-circuit (floating)
- Connect VSS_RTC to VSS

If no crystal oscillator or LVCMOS clock source is used then:

- Connect the RTC_OSC_XI_CLKIN32 terminal through a pull-down resistor to VSS
- Leave the RTC_OSC_XO terminal open-circuit (floating)
- Connect VSS_RTC to VSS

If the RTC is not used, see [Section 2.19](#).

2.8 System Issues

2.8.1 Pull-Up/Pull-Down Resistors

Ensure all pullups connected to AM57xx devices are pulled up to the correct I/O voltage to avoid any leakage between the I/O rails of the device. Each terminal has an associated supply name used to power its I/O cell. This can be found in the *Ball Characteristics* table in the AM57xx device-specific data manual. For example, if you want to pull up terminal SPI1_CS1 in any mux mode (spi1_cs1, sata1_led, spi2_cs1, gpio7_11, and so forth), the signal must be pulled up to VDDSHV3.

Some pins may have internal pull-up or pull-down resistors enabled while the device is held in reset. In cases where external pull resistors conflict with internal pull resistors, the conflict may create a voltage offset on the associated pins until reset is released and the pad configuration registers are programmed to disable conflicting internal resistors. System initialization software should disable internal resistors as soon as possible for pins with conflicting external resistors to minimize the exposure time to this offset. Additionally, for output-only pins, you can disable the RX portion of the pad cell to eliminate this leakage.

2.8.2 Peripheral Clock Outputs

Put 22 Ω series resistors (close to processor) on the output clocks of the following modules: MMC, GPMC, McASP (both clock and frame sync), SPI, QSPI and VOUT.

2.8.3 General Debug

Output clocks CLKOUT1, CLKOUT2, and CLKOUT3 are present on several of the pins. If these pins/signals are not used in your design, it is good to have test points on these signals to be able to monitor internal clocks to support hardware and software debugging.

2.9 Low Power Considerations

If you are designing for low power, here are some tips to help you optimize your design for low power:

- On early prototype boards, it is recommended to include small shunt resistors in the voltage rail paths of each of the following power rails of AM57xx device: VDD_MPU, VDD, VDDS_DDR1, VDDS_DDR2, VDD_DSPEVE, VDD_IVA, VDD_GPU, VDDSHV1-11. These are listed in order of priority. If you cannot isolate them all, then the most important ones are the core rails listed first. Also, the VDDSHVx supplies may be broken into multiple segments and may be run at different voltages (VDDSHV8 for the microSD card can switch 3.3 V/1.8 V mode at run-time but the others cannot). This will help you measure the power consumption of each rail and potentially pinpoint high power consumption during development. You may also want to add these shunt resistors for power supplies connected to other devices to be able to measure power on those key devices. The AM57xx EVMs have examples of these shunt resistors.
- For production, these shunt resistors must be removed from the design (turned into a continuous plane) since these resistors restrict current flow and add inductance to the PDN.

2.10 Clocking

- If you do not need the RTC timer feature, you do not need to include a 32 KHz crystal. The 32 KHz reference can come from the high frequency clock or onboard RC oscillator. RTC_OSC_XI_CLKIN32 should be connected to VSS. Leave the RTC_OSC_XO pin not connected (floating). For more information, see [Section 2.19](#).
- When using an external crystal, connect VSS_OSC to board ground.
- It is preferable to always have bias and dampening resistors that can help tune the crystal later. For more information, see the *Input Clock Specifications* section of the device-specific data manual.

2.11 DDR3

- It is very important to follow the DDR3 routing guidelines in the AM57xx device-specific data manual. These guidelines are very important to ensure a proper DDR3 operation.
- When using a resistor divider for DDR_VREF, ensure resistors are high precision resistors (1% or better) as specified in the data manual.
- Provide adequate decoupling capacitors on the DDR power rails both at the AM57xx device as well as at the DDR SDRAM device(s). Proper distribution of these capacitors is mandatory. They must be located at both the AM57xx device's DDR interface and at the SDRAMs near the trace ends when routing fly-by nets adjacent to the DDR_VDDsx power plane.
- Designs with point to point connections between the AM57xx devices and a single DDR3 SDRAM typically do not need VTT termination, although, this may be needed depending on the specific PCB characteristics. For multiple device topologies or multi-die packages, VTT termination is required. A VTT termination regulator is required for properly terminating the address, command and control fly-by signals. For a proper connection, see the device-specific data manual. The [TPS51200](#) or [TPS51206](#) are recommended for use as the VTT termination regulator.
- Do not connect DDR_RESET to VTT termination resistors. DDR_RESET should be connected directly between the AM57xx devices and the SDRAMs. Addition of a pull-down resistor is also recommended.

- For proper termination voltages, see the device-specific data manual. Termination for the fly-by clock signals is to VDDS_DDR1 and VDDS_DDR2 (through termination resistors to a balancing coupling capacitor), whereas, all other fly-by signals need to use terminations resistors connected to VTT for the termination voltage. For more information, see the device-specific data manual.
- VREF can be obtained from the VTT termination regulator or from a resistor divider (2.2K Ω 1% resistors) with capacitive decoupling to ground. It will be used as references for both CA and DQ pins on the memory, as well as the VREF signal on the AM57xx devices. Ensure resistors are high precision (1% or better) resistors as specified in the device-specific data manual. Be sure to carefully follow the VREF routing guidelines in the device-specific data manual.
- ECC is supported on EMIF1 but its use is currently limited to specific implementations. For more information, see the device-specific errata document.
- Data bit swapping within the data byte is allowed. The PHY is implemented such that this does not impact leveling. Bit swapping is not allowed for any other group of signals, including ADDR and CNTL.
- Address mirroring (as defined in JEDEC DDR3 documentation) is not supported on this device. The device-specific data manual refers to a mirrored placement, which means that the SDRAM devices can be mounted on both top and bottom. This is allowed as long as the routing rules are still met, which takes significant care. The reference to 'mirrored placement' does not mean that 'address mirroring' is supported.
- If a particular DDR interface is not used, then the applicable DDRx_DQSn and DDRx_DQSNn pins should be pulled to GND or to the appropriate power supply through a 1K Ω resistor to keep the signals inactive as stated in the device-specific data manual. The same is also required if only a single byte lane is unused, such as the ECC byte lane. The address, command, control, clock and data lines can all be left floating. The DDR supplies and VREF must be maintained at their rated levels per the device-specific data manual.

2.12 MMC

- Include a 22 Ω series resistor on MMCx_CLK (as close to the processor as possible). This signal is used as an input on read transactions and the resistor eliminates possible signal reflections on the signal that can cause false clock transitions.
- For SD-CARD implementations, 10K pull-up resistors are needed on all data signals and on the command signal.
- For eMMC implementations, 47K-50K pull-up resistors are only needed on the first data signal (DAT0) and on the command signal. They are not required on the DAT7:DAT1 connections as these are provided within the eMMC device at start-up.
- To support the UHS-I speeds on MMC1,
 - You need a dedicated, configurable LDO connected to VDDSHV8. The EVM uses the LDO1 output from the PMIC.
 - Do not use this LDO to power anything else on the board since it will change dynamically at run-time.
 - The SD card's VDD signal should be connected to a fixed 3.3 V rail. In other words, the card's VDD must remain at 3.3 V even for the UHS-I modes of operation. Only the signaling levels change in these modes, not VDD.
 - Pullups on the SD/MMC signals should go to the LDO rail such that their voltages coincide with the mode of operation.

2.13 I2C

- Pull-up resistors must be attached on both I2C signals (I2C_DATA and I2C_CLK). The value on each should be between 2.2K and 4.7K. Use of the 2.2K pull-up resistor decreases the signal rise time and increases noise immunity at the expense of increased current dissipation. Ensure the pull-up resistors connect to the correct I/O voltage rail, see [Section 2.8.1](#). If using floating gate level translators on the I2C bus, make sure that the combined pull-up resistance for all pull-up resistors on each signal result in a composite resistance between 2.2K and 4.7K.
- If you are planning to use TI's software, be sure to connect I2C1 to the PMIC, as this is the port used for PMIC control.
- I2C1 and I2C2 use true open drain buffers that are fully compliant to the I2C specifications. These support 100 kHz and 400 kHz operation.
- I2C3/4/5 use LVCMOS buffers to emulate an open drain buffer. These can support 3.4 Mbps I2C operation. However, these ports are not fully compliant with the I2C specs. In particular the falling edges are too fast (<2 ns). Any devices connected to these ports must be able to function properly with this fall time.

2.14 QSPI

- Make sure SCLK is looped back at the board level to RTCLK in order to leverage the faster mode 0 timings.
- Be sure that D0 of the QSPI peripheral connects with D0 of the memory. The initial communication occurs only over D0 and the interface will not work if these are not connected.
- Follow the layout guidelines in the device-specific data manual.

2.15 NAND

- Typically the R/B# signal from the NAND is open drain and connected to the AM57xx GPMC_WAIT signal. Be sure to include a 4.7K pullup to the appropriate voltage, depending whether the NAND is 1.8 V or 3.3 V.

2.16 VOUT

- VOUT3 on AM572x devices must only be operated at 1.8 V when it is multiplexed onto the VIN1A pins in the VDDSHV6 power domain. Alternately, use VOUT3 at 3.3 V when it is multiplexed onto the GPMC pins in the VDDSHV10 power domain. For more information, see the [AM572x Sitara™ Processors Silicon Revision 2.0, 1.1 Silicon Errata](#).
- VOUT1, VOUT2 and VOUT3 on AM571x devices must only be operated at 1.8 V. For more information, see the [AM571x \(SR 2.0, 1.0\) and AM570x \(SR 2.1, 2.0\) Sitara™ Processors Silicon Errata](#).
- VOUT1, VOUT2 and VOUT3 on AM570x and AM574x devices may be operated at 3.3 V or 1.8 V without restriction.

2.17 USB

- For detailed recommendations on proper USB signal connection and routing, see the [High-Speed Interface Layout Guidelines](#).
- For USB Device operation, USB VBUS decoupling capacitance should be < 10 μF.
- For USB Host operation, USB VBUS decoupling capacitance should be > 120 μF.
- Ensure the VBUS decoupling capacitance is connected close to USB connector.
- USBx_DP and USBx_DM should never have any series resistors or capacitance on these signals. These signals should be straight traces to the connector with no stubs or test points.
- Typical connections of the AM57xx for a USB Device:
 - USBx_DP and USBx_DM are connected directly to the USB connector
 - Connector ID pin can be left unconnected
 - USBx_DRVVBUS is not used and can be left unconnected

- Typical connections of the AM57xx for a USB Host:
 - USBx_DP and USBx_DM are connected directly to the USB connector
 - Connector ID should be grounded
 - USBx_DRVVBUS should be connected to the enable of the 5 V VBUS power source
 - Connector VBUS should be connected to the output of the 5 V VBUS power from the power switch by USBx_DRVVBUS
- Typical connections for a USB Host with USB hub:
 - USBx_DP and USBx_DM are connected directly to the USB hub upstream port (hub then distributes these signals to the downstream ports as needed)
 - Connector ID should be grounded to enable host mode
 - USBx_DRVVBUS should be unconnected
 - USBx_VBUS should be connected to the output of the 5 V VBUS power source. It is also connected to the VBUS detect on the hub, which then allows the hub to selectively enable or disable typically through a power switch to each downstream port.
- Common-mode chokes may be needed for EMI/EMC control. Note that these may reduce the signal amplitude and degrade performance.

2.18 Ethernet

- No series resistors are required for MII signals. They may be implemented on the clock signals if the routes are long or through a connector.
- For the RGMII interfaces, 22 Ω series termination resistors must be placed on all 12 interface signals as close to the transmitting I/O a possible. Be sure to check voltage compatibility between the AM57xx I/O and the Ethernet PHY I/O.
- Some Ethernet PHYs use their output data pins (named as RX) to latch the default operating state. In many cases these pins are connected to AM57xx input pins that have internal pull resistors which may conflict with external pull resistors. Alternately, the Ethernet PHY configuration technique may use voltages that are not valid LVCMOS levels. These conditions will cause voltage offsets until the associated signals are driven or conflicting internal resistors are disabled by software. System initialization software should disable internal resistors and initialize the PHY as soon as possible after reset release to minimize the time these conditions exist.

2.19 RTC

Table 2 describes what to do with each pin related to RTC functionality. Two use case scenarios are provided:

- RTC timer functional: If you will be using the RTC feature, this use case allows you to use the Real Time Clock features (keeping time).
- RTC feature disabled: If you will never use the RTC features, the RTC functions are fully disabled.

Table 2. Proper RTC Connections

Pin ⁽⁵⁾	Function	RTC Timer Functional	RTC Feature Disabled
VDD_RTC ⁽¹⁾	1.06 V power supply	AM57xx VDD power supply	AM57xx VDD power supply
VDDA_RTC ⁽²⁾	1.8 V power supply	vdds18v	vdds18v
RTC_ISO ⁽²⁾	RTC domain isolation signal	PORZ	PORZ
RTC_PORZ ⁽³⁾	RTC power on reset input	PORZ	VSS
EXT_WAKEUP0 ⁽⁴⁾	External wakeup input 0	Pull-down to VSS	Pull-down to VSS
EXT_WAKEUP1 ⁽⁴⁾	External wakeup input 1	Pull-down to VSS	Pull-down to VSS
EXT_WAKEUP2 ⁽⁴⁾	External wakeup input 2	Pull-down to VSS	Pull-down to VSS
EXT_WAKEUP3 ⁽⁴⁾	External wakeup input 3	Pull-down to VSS	Pull-down to VSS

- (1) If using an external LVCMOS input for the 32 kHz clock, it must be amplitude of VDDA_RTC since this pin is related to VDDA_RTC power domain.
- (2) RTC_ISO, RTC_PORZ and the WAKEUPx signals are all on the VDDSHV5 power domain. Since the VDDSHV5 power domain can be either 1.8 V or 3.3 V, nominal, these signals must be driven from sources of the matching VDDSHV5 level.
- (3) PORZ is on the VDDSHV3 power domain. The recommendation to connect RTC_ISO to PORZ is valid only if VDDSHV5 and VDDSHV3 are powered by equal voltage levels (3.3 V or 1.8 V). Alternately, when unused, RTC_ISO can be pulled up to VDDSHV5. Similarly, if PORz and RTC_PORz are at different voltages, appropriate level versions of each need to be provided.
- (4) WAKEUPx pins that are configured for other pinmux options do not need to be terminated per this table. These recommendations are for when they are configured for WAKEUP pin functionality.
- (5) Power supplies listed in this table must be sequenced according to the diagrams in the device-specific data manual.

2.20 JTAG and EMU

- Clock and signal buffering are required whenever the JTAG interface connects to more than one device. Clock buffering is strongly recommended even for single device implementations. Verify series terminations are provided on each clock buffer output and ideally, that the clock output tracks are skew matched.
- EMU pins must not be buffered. EMU[1:0] can be bussed to multiple devices. Other EMU pins connected for trace usage must be short and skew matched.
- For more recommendations on EMU routing, see [Emulation and Trace Headers Technical Reference Manual](#).
- Similarly, a summary of this information is available in the [XDS Target Connection Guide](#).
- Adaptive clocking must be implemented correctly using the RTCK output.
- If the JTAG and EMU interface is not used, all pins except TRSTn, TCK and TMS can be left floating. TRSTn must be pulled low to ground through a 4.7kΩ resistor. TCK and TMS must be pulled to VDDSHV3 through a 4.7kΩ resistor. However, it is strongly recommended that all board designs contain at least a minimal JTAG port connection to test points or a header footprint to support early prototype debugging. The minimum connections are TCK, RTCK, TMS, TDI, TDO and TRSTn. JTAG routes and component footprints (except the PD on TRSTn and the PU on TMS and TCK) can be deleted in the production version of the board, if desired.
- In the event that the JTAG interface is used and the EMU interface (or a subset of the emulation pins) is not used, the unused EMU pins can be left floating.

2.21 PCIe

- For detailed recommendations for proper PCIe signal connection and routing, see the [High-Speed Interface Layout Guidelines](#).
- DC blocking caps are needed on the reference clock input.
- DC blocking capacitors are required for data lanes and should be implemented adjacent to the TX pins of the AM57xx device.

2.22 GPIO

- There are some GPIO pins that are input-only:
 - gpio1_0
 - gpio1_1
 - gpio1_2
 - gpio1_3
 - gpio8_27
- Occasionally, GPIO pins are configured as outputs that drive high current steady-state loads which may result in a VOH or VOL level that is held away from the supply rail. In these cases, the receiver associated with these pins should be disabled to minimize VDD to VSS leakage through the input buffer. Alternately, external buffers can be implemented to prevent this condition.

3 References

- Texas Instruments: [AM572x Sitara™ Processors Silicon Revision 2.0 Data Manual](#)
- Texas Instruments: [AM571x Sitara™ Processors Silicon Revision 2.0 Data Manual](#)
- Texas Instruments: [AM570x Sitara™ Processors Data Manual](#)
- Texas Instruments: [AM574x Sitara™ Processors Silicon Revision 1.0 Data Manual](#)
- Texas Instruments: [AM572x Sitara™ Processors Silicon Revision 2.0, 1.1 Silicon Errata](#)
- Texas Instruments: [AM571x \(SR 2.0, 1.0\) and AM570x \(SR 2.1, 2.0\) Sitara™ Processors Silicon Errata](#)
- Texas Instruments: [AM574x Sitara™ Processors Silicon Revision 1.0 Silicon Errata](#)
- Texas Instruments: [AM574x, AM572x, and AM571x Compatibility Guide](#)
- Texas Instruments: [High-Speed Interface Layout Guidelines](#)
- Texas Instruments: [AM57xx BGA PCB Design](#)
- Texas Instruments: [AM572x General Purpose EVM Hardware User's Guide](#)
- [AM57xx PCB Escape Routing Guidelines](#) wiki
- [TI PinMux Tool](#) wiki
- [AM572x Evaluation Module](#)
- [AM572x Industrial Development Kit \(IDK\)](#)
- [AM571x Industrial Development Kit \(IDK\)](#)
- [DRA71x Evaluation Module](#)
- [AM570x 6-Layer PCB Reference Design](#)
- [AM574x Industrial Development Kit \(IDK\)](#)
- Texas Instruments: [TPS659037 Design Guide](#)
- Texas Instruments: [TPS659037 Design Checklist](#)
- Texas Instruments: [TPS659037 User's Guide to Power AM574x, AM572x, and AM571x User's Guide](#)
- Texas Instruments: [TPS65916 User's Guide to Power AM571x User's Guide](#)
- Texas Instruments: [LP87332D and LP873220 User's Guide to Power AM570x User's Guide](#)
- Texas Instruments: [TPS65916 User's Guide to Power AM5 User's Guide](#)
- Texas Instruments: [Emulation and Trace Headers Technical Reference Manual](#)

- Texas Instruments: [XDS Target Connection Guide](#)
- Texas Instruments: [Powering the AM335x With the TPS650250](#)
- Texas Instruments: [AM574x Sitara™ Processors Silicon Revision 1.0 Technical Reference Manual](#)
- Texas Instruments: [AM572x Sitara™ Processors Silicon Revision 2.0, 1.1 Technical Reference Manual](#)
- Texas Instruments: [AM571x \(SR2.0, SR1.0\) AM570x \(SR2.1, SR2.0\) Sitara™ Processors Technical Reference Manual](#)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (April 2019) to B Revision	Page
• Updates were made in Section 2.8.1	7
• Updates were made in Section 2.12	9
• Updates were made in Section 2.13	10
• Update was made in Section 2.18	11
• Update was made in Section 2.22	13

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