# AS1339

## 650mA RF Step-Down DC-DC for PA, with two LDOs

## 1 General Description

The AS1339 is a high-frequency step-down converter optimized for dynamically powering the power amplifier (PA) in WCDMA or NCDMA handsets. The device uses a 110mΩ typical bypass FET to power the PA directly from the battery during high-power transmission. The IC integrates two 10mA low-noise, low-dropout regulators (LDOs) for PA biasing.

With a switching frequency of 2MHz, the device allows optimization for smallest solution size or highest efficiency. The AS1339 supports fast switching using small ceramic 10µF input and 4.7µF output capacitors to maintain low ripple voltage.

The AS1339 uses an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The gain from REFIN to OUT is 2.5V/V. At high-duty cycle, the device automatically switches to a bypass mode, connecting the input to the output through a low-impedance MOSFET. The LDOs are designed for low-noise operation, wherein each LDO in the device is individually enabled through its own logic control interface. The device is available in a 16-pin WLP (2x2mm) package.

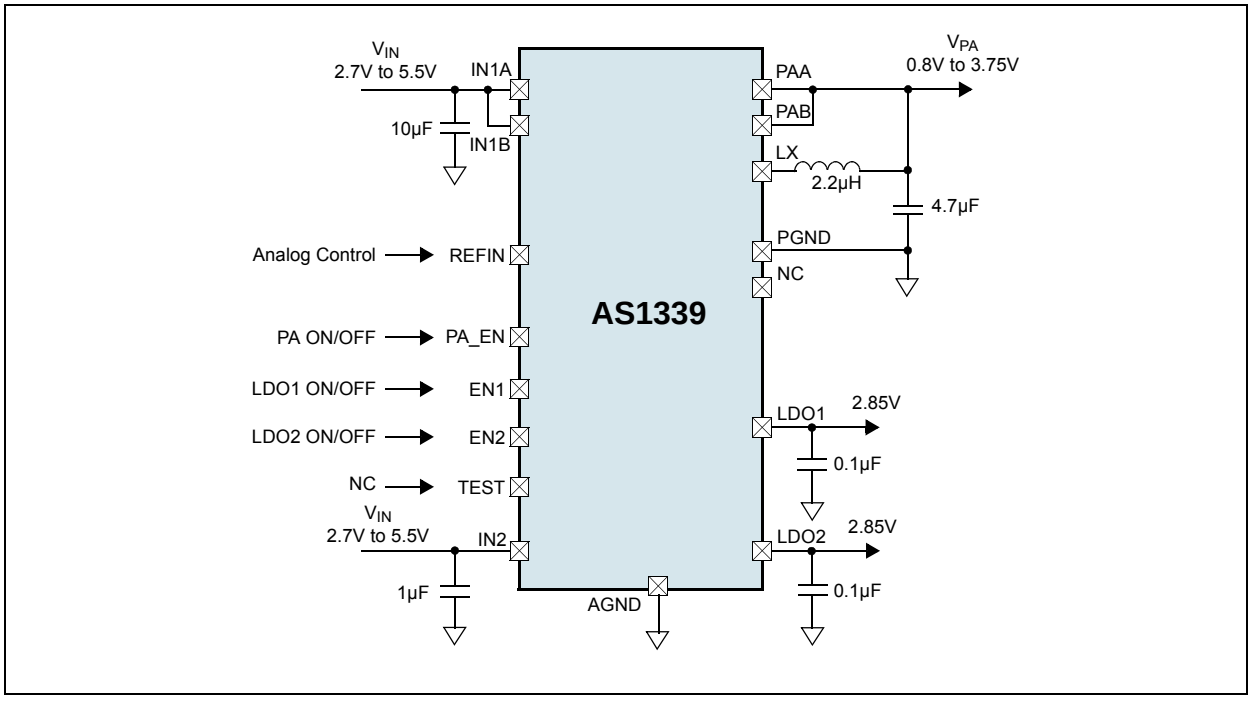
## 2 Key Features

- Fixed Switching Frequency: 2MHz
- PA Step-Down Converter
- Low Dropout Voltage
- Low Output-Voltage Ripple
- Dynamic Output Voltage Control (0.8V to 3.75V)
- 30µs Settling Time for 0.8V to 3.4V Output Voltage Change
- 650mA Output Drive Capability
- Two 10mA Low-Noise LDOs
- Low Shutdown Current
- Supply Voltage Range: 2.7V to 5.5V
- Thermal Shutdown
- 16-pin WLP (2x2mm) package

## 3 Applications

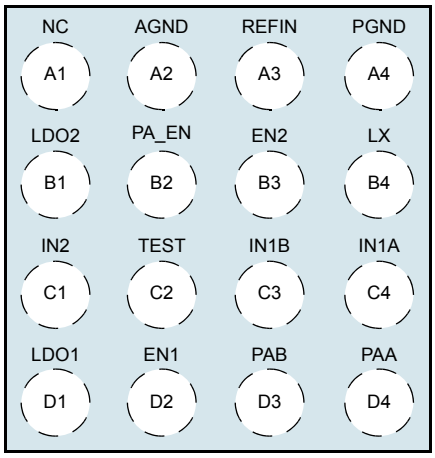
The AS1339 is ideal for WCDMA/NCDMA cellular handsets, Wireless PDAs, and Smartphones.

*Figure 1. AS1339 - Typical Operating Circuit*



# 4 Pinout

*Figure 2. Pin Assignments (Top View)*




## Pin Description

*Table 1. Pin Description*

| Pin Name | Pin Number | Description |
|---|---|---|
| NC | A1 | **Not Connected.** Free, high impedance for normal operation. Used for internal test purpose. |
| AGND | A2 | **Low-Noise Analog Ground** |
| REFIN | A3 | **DAC-Controlled Input.** Reference voltage for buck converter. The output of the PA step-down converter is regulated to 2.5 x $V_{REFIN}$. Bypass mode is enabled when $V_{IN} \leq 2.69V \times V_{REFIN}$. |
| PGND | A4 | **Power Ground** for PA Step-Down Converter |
| LDO2 | B1 | **10mA LDO Regulator 2 Output.** Connect LDO2 with a 0.1µF ceramic capacitor as close as possible to LDO2 and AGND. LDO2 is internally pulled down through a 100Ω resistor when this regulator is disabled. |
| PA_EN | B2 | **PA Step-Down Converter Enable Input.** For normal operation, connect to logic-high. For shutdown mode, connect to logic-low. The pin is internally pulled down through a 110kΩ resistor. |
| EN2 | B3 | **Enable Input for LDO2.** For normal operation, connect to logic-high. For shutdown mode, connect to logic-low. The pin is internally pulled down through a 110kΩ resistor. |
| LX | B4 | **Inductor Connection.** Connect an inductor from LX to the output of the PA step-down converter. |

*Table 1. Pin Description*

| Pin Name | Pin Number | Description |
|---|---|---|
| IN2 | C1 | **Supply Voltage Input for LDO1 and LDO2.** Connect IN2 to a battery or supply voltage from 2.7V to 5.5V. Decouple IN2 with a 1µF ceramic capacitor as close as possible to IN2 and AGND. Connect IN2 to the same source as IN1A and IN1B. |
| TEST | C2 | **NC.** Used for internal test purpose. The pin is internally pulled down with a 110kΩ resistor. |
| IN1B, IN1A | C3, C4 | **Supply Voltage Input for PA Step-Down Converter.** Connect IN1A/B to a battery or supply voltage from 2.7V to 5.5V. Decouple IN1A/B with a 10µF ceramic capacitor as close as possible to IN1A/B, and PGND. IN1A and IN1B are internally connected together. Connect IN1A/B to the same source as IN2. |
| LDO1 | D1 | **10mA LDO Regulator 1 Output.** Decouple LDO1 with a 0.1µF ceramic capacitor as close as possible to LDO1 and AGND. LDO1 is internally pulled down through a 100Ω resistor when this regulator is disabled. |
| EN1 | D2 | **Enable Input for LDO1.** For normal operation, connect to logic-high. For shutdown mode, connect to logic-low. The pin is internally pulled down through a 110kΩ resistor. |
| PAB, PAA | D3, D4 | **PA Connection for Bypass Mode.** Internally connected to IN1A/B using the internal bypass MOSFET during bypass mode. Connect PAA/B with a 4.7µF ceramic capacitor as close as possible to PAA/B and PGND. |

# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|
| IN1A, IN1B, IN2 to AGND | -0.3 | +7 | V | |
| PAA, PAB, PA_EN, TEST, REFIN, NC to AGND | -0.3 | $V_{IN1A}$/ $V_{IN1B}$ + 0.3 | V | |
| LDO1, LDO2, EN1, EN2 to AGND | -0.3 | $V_{IN2}$ + 0.3 | V | |
| REFIN Common-Mode Range | 0 | $V_{IN}$ | V | |
| IN2 to IN1B/IN1A | -0.3 | +0.3 | V | |
| PGND to AGND | -0.3 | +0.3 | V | |
| LX Current | | 0.8 | $A_{RMS}$ | |
| Bypass Current | | 1.6 | $A_{RMS}$ | |
| Human Body Model | 1 | | kV | *HBM MIL-Std. 883E 3015.7* methods |
| Storage Temperature Range | -65 | +150 | ºC | |
| Package Body Temperature | | +260 | ºC | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* |
| Continuous Power Dissipation $P_{D-MAX}$ | | 0.75 | W | $T_A$ = +65ºC; derate 12.5mW/ºC above +65ºC |
| Junction Temperature ($T_J$) Range | -40 | +125 | ºC | |
| Ambient Temperature ($T_A$) Range | -40 | +85 | ºC | In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$. |

# 6 Electrical Characteristics

*$V_{IN1A}$ = $V_{IN1B}$ = $V_{IN2}$ = $V_{PA\_EN}$ = $V_{EN1}$ = $V_{EN2}$ = 3.6V, $T_A$ = -40ºC to +85ºC. Typical values are at $T_A$ =+25ºC, (unless otherwise specified), for external components refer to Table 5 on page 7.*

*Table 3. Electrical Characteristics*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input Supply** | | | | | | |
| $V_{IN}$ | Input Voltage Range | | 2.7 | | 5.5 | V |
| $I_{SHDN}$ | Shutdown Supply Current | $V_{PA\_EN}$ = $V_{EN1}$ = $V_{EN2}$ = 0V[1] | | 0.1 | 1 | µA |
| $I_Q$ | DC-DC No-Load Supply Current | $V_{EN1}$ = $V_{EN2}$ = 0V, $I_{LOAD(DCDC)}$ = 0mA, switching, $V_{IN}$ = 4.5V, $V_{OUT}$ = 3.4V | | 4.5 | 6 | mA |
| **DCDC Output Voltage** | | | | | | |
| $I_{LOAD}$ | Load Current | | | | 650 | mA |
| $V_{OUT}$ | Output Voltage Range | PWM Mode | 0.8 | | 3.85 | V |
| | Output Voltage | $V_{REFIN}$ = 0.32V, $V_{IN}$ = 3.9V | 0.75 | 0.8 | 0.85 | V |
| | | $V_{REFIN}$ = 0.84V, $V_{IN}$ = 3.9V | 2.05 | 2.1 | 2.15 | V |
| | | $V_{REFIN}$ = 1.36V, $V_{IN}$ = 3.9V | 3.319 | 3.4 | 3.481 | V |
| **Thermal Protection** | | | | | | |
| | Thermal Shutdown | $T_A$ rising, 10ºC typical hysteresis | | +140 | | ºC |
| **Logic Control** | | | | | | |
| | PA_EN, EN1, EN2, Logic-Input High Voltage | 2.7V ≤ $V_{IN}$ ≤ 5.5V | 1.4 | | | V |
| | PA_EN, EN1, EN2, Logic-Input Low Voltage | 2.7V ≤ $V_{IN}$ ≤ 5.5V | | | 0.5 | V |
| | Logic-Input Current (PA_EN, EN1, EN2) | $V_{IL}$ = 0V | -1 | | +1 | µA |
| | | $V_{IH}$ = $V_{IN}$ = 5.5V | | 50 | 75 | µA |
| **REFIN** | | | | | | |
| | REFIN Operating Common-Mode Range | | 0.32 | | 1.5 | V |
| | REFIN gain $V_{OUT}/V_{REFIN}$[2] | $V_{REFIN}$ = 0.32V | 2.35 | 2.50 | 2.65 | V/V |
| | | $V_{REFIN}$ = 0.84V, 1.36V | 2.44 | 2.50 | 2.56 | V/V |
| | REFIN Current | $V_{REFIN}$ = $V_{IN}$ = 5.5V | -1 | | +1 | µA |
| **LX** | | | | | | |
| $R_{DSONP}$ | Pin-Pin Resistance for PFET | $I_{SW}$ = 200mA; $T_A$ = +25°C | | 110 | 200 | mΩ |
| | | $I_{SW}$ = 200mA | | | 230 | |
| $R_{DSONN}$ | Pin-Pin Resistance for NFET | $I_{SW}$ = -200mA; $T_A$ = +25°C | | 230 | 415 | mΩ |
| | | $I_{SW}$ = -200mA | | | 485 | |
| | PFET Leakage Current | $V_{IN}$ = 5.5V, $V_{LX}$ = 0V | | 0.1 | 3 | µA |
| | NFET Leakage Current | $V_{IN}$ = $V_{LX}$ = 5.5V | | 0.1 | 3 | µA |
| | PFET Peak Current Limit | $V_{LX}$ = 0V | | 1100 | | mA |

*Table 3. Electrical Characteristics (Continued)*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC}$ | Internal Oscillator Frequency | | 1.8 | 2 | 2.2 | MHz |
| **BYPASS** | | | | | | |
| | Bypass Activation Factor | $V_{REFIN}$ rising, 50mV hysteresis | 2.56 | 2.69 | 2.78 | V/V |
| | On-Resistance Bypass PFET | $I_{SW}$ = 200mA; $T_A$ = +25°C | | 110 | 200 | mΩ |
| | | $I_{SW}$ = 200mA | | | 230 | |
| | PFET Bypass Off-Leakage Current | $V_{IN}$ = 5.5V, $V_{PAA}$ = $V_{PAB}$ = 0V | | 0.1 | 3 | µA |
| **LDO1/2** | | | | | | |
| | Output Voltage | $I_{OUT}$ = 0mA, 10mA; | 2.75 | 2.85 | 2.95 | V |
| | Quiescent Current | one LDO enabled, $I_{OUT}$ = 0mA | | 25 | 50 | µA |
| | | both LDOs enabled, $I_{OUT}$ = 0mA | | 40 | 80 | |
| | Output Current | | 10 | | | mA |
| | Current Limit | $V_{OUT}$ = 0V | 20 | 35 | 50 | |
| | Dropout Voltage[3] | $I_{OUT}$ = 10mA | | 20 | 50 | mV |
| $R_{OFF}$ | Shutdown Output Impedance | $V_{EN1/2}$ = 0V | | 100 | | Ω |

1. Current into supply pins without leakage of DCDC switches.
2. Limited by the 50mV output voltage accuracy for $V_{REFIN}$ < 0.84V
3. The dropout voltage is the input to output difference at which the output is 100mV below its nominal value.

## System Characteristics

*$V_{IN1A}$ = $V_{IN1B}$ = $V_{IN2}$ = $V_{PA\_EN}$ = $V_{EN1}$ = $V_{EN2}$ = 3.9V, $T_A$ = -40ºC to +85ºC. Typical values are at $T_A$ =+25ºC, (unless otherwise specified), for external components refer to* Table 5 on page 7. The following parameters are verified by characterisation and are not production tested.

*Table 4. System Characteristics*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **REFIN** | | | | | | |
| | REFIN gain variation; relative linearity[1] | 0.32V ≤ $V_{REFIN}$ ≤ 1.4V | | | 3 | % |
| | REFIN gain variation; absolute linearity[2] | 0.84V ≤ $V_{REFIN}$ ≤ 1.4V | -2.4 | | 2.4 | % |
| | | 0.32V ≤ $V_{REFIN}$ ≤ 0.84V | -50 | ±10 | 50 | mV |
| **LX** | | | | | | |
| | Ripple voltage, PWM mode[3] | $V_{OUT}$ = 0.8 to 3.4V, $R_{LOAD}$ = 8Ω, no bypass mode, no pulse-skip condition | | 10 | 25 | mVp-p |
| Line_tr | Line transient response | $V_{IN}$ = 3.4 to 3.9V, $V_{OUT}$ = 3.0V, $I_{OUT}$ = 300mA, $V_{IN}$ increase 300mV in 10µs | | 30 | 50 | |
| Load_tr | Load transient response | $V_{IN}$ = 3.4 to 4.2V, $V_{OUT}$ = 3.0V, $T_{RISE}$ = $T_{FALL}$ = 10µs, $I_{OUT}$ = 100 to 300mA | | 50 | 70 | |

*Table 4. System Characteristics (Continued)*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Start-Up Time | From PA_EN switch from 0V to 1.7V, VOUT = 3.4V, ILOAD = 0mA, within 50mV regulation error | | 100 | 150 | µs |
| | Regulation Time; Rise Time | VOUT from 0.8V to 3.4V, RLOAD = 8Ω, within 50mV regulation error | | 30 | 50 | |
| | Regulation Time; Fall Time | VOUT from 3.4V to 0.8V, RLOAD = 8Ω, within 50mV regulation error | | 30 | 50 | |
| **LDO** | | | | | | |
| | Start-Up Time | IOUT=10mA, within 100mV of VOUT | | 30 | 50 | µs |
| | Shut-Down Time | IOUT=0mA, within 100mV of GND | | 50 | 100 | |
| | Line Regulation[4] | VIN = 4V to 3.5V; IOUT = 10mA; | | | 10 | mV |
| | Load Regulation | IOUT stepped from 50µA to 10mA | | | 25 | |
| | Ripple Rejection[5] | IOUT = 4mA, VIN = 3.2V, f = 100kHz | 45 | | | dB |
| | | IOUT = 4mA, VIN = 3.2V, f = 2MHz | 45 | | | |
| | Output Noise[6] | 10Hz to 100kHz, IOUT = 10mA | | 50 | 100 | µVRMS |

1. The relative linearity is defined as the difference of the minimum to the maximum gain over the entire REFIN range.
2. The absolute linearity is defined as the actual gain error (AE) of every applied VREFIN voltage between 0.32V and 1.4V.

$$AE = \left(\frac{V_{OUT}}{2,5 \times V_{REFIN}} - 1\right) \times 100$$

3. The ripple voltage should measured at $C_{OUT}$ electrode on good layout PC board and under condition using suggested inductors and capacitors.
4. For dynamic change in VOUT (Line transient response) when VIN drops 500mV from 4V (see Figure 48 on page 15); Slew rate= 40mV/µs.
5. VRIPPLE = 200mVpp; TA = +25°C; CIN1, CIN2 removed; PA_EN = 0V;
6. VIN = 3.2V; TA = +25°C; PA_EN = 3.2V;

*Table 5. External Components used for Characterisation*

| Name | Part Number | Value | Rating | Type | Size | Manufacturer |
|---|---|---|---|---|---|---|
| CIN1 | GRM21BR60J106KE01 | 10µF | 6.3V | X5R | 0805 | Murata www.murata.com |
| CIN2 | GRM155R61A105KE15 | 1µF | 10V | X5R | 0402 | |
| COUT | C0603C475K8PAC7867 | 4.7µF | 10V | X5R | 0603 | KEMET www.kemet.com |
| CLDO1, CLDO2 | C0402C104K4RAC | 100nF | 16V | X7R | 0402 | |
| L | MLP2520S3R3S | 3.3µH | 1A | 110mΩ | 2.2x2.0x1.4mm | TDK www.coilcraft.com |

# 7 Typical Operation Characteristics

*Figure 3. DC-DC Efficiency vs. VOUT; RLOAD = 5Ω*

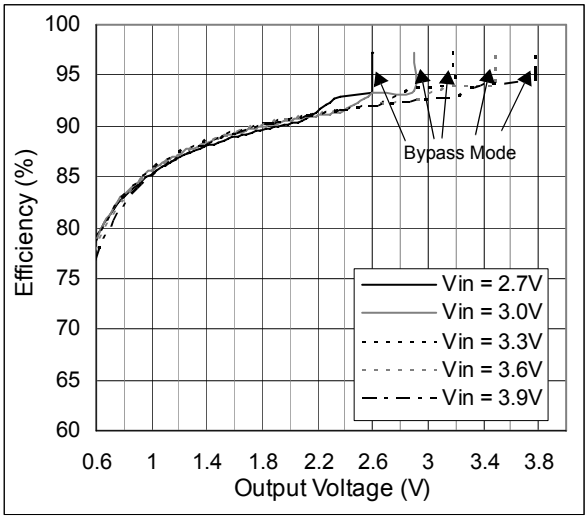



*Figure 4. DC-DC Efficiency vs. VOUT; RLOAD = 7.5Ω*

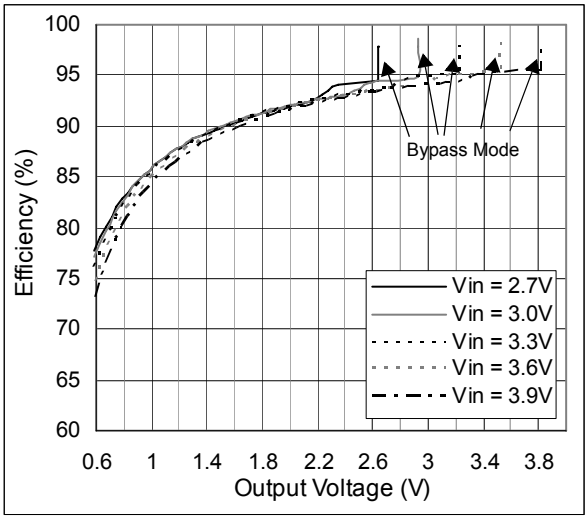



*Figure 5. DC-DC Efficiency vs. VOUT; RLOAD = 10Ω*

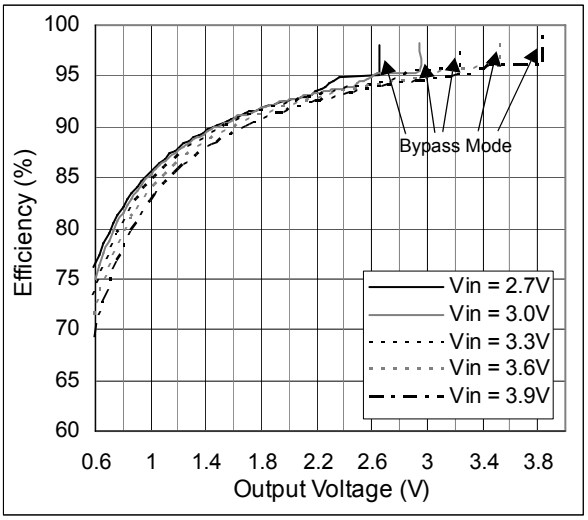



*Figure 6. DC-DC REFIN vs. VOUT; RLOAD = 5Ω*

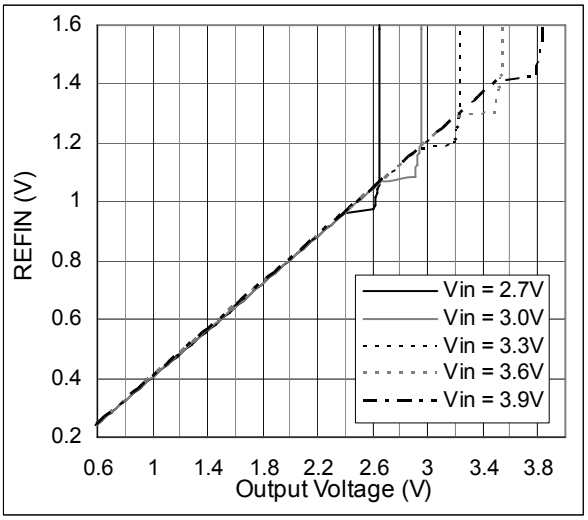



*Figure 7. DC-DC REFIN vs. VOUT; RLOAD = 7.5Ω*

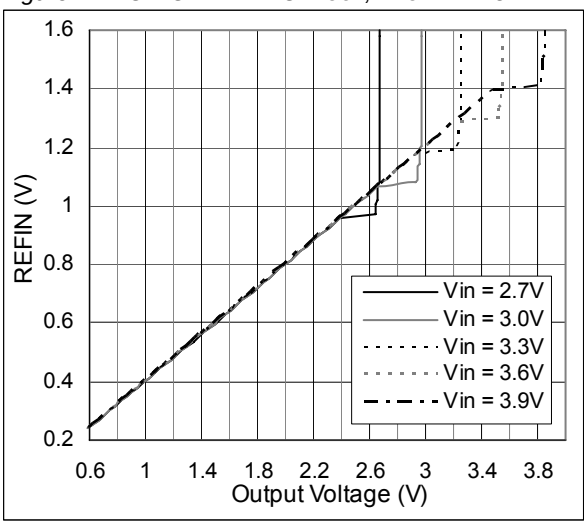



*Figure 8. DC-DC REFIN vs. VOUT; RLOAD = 10Ω*

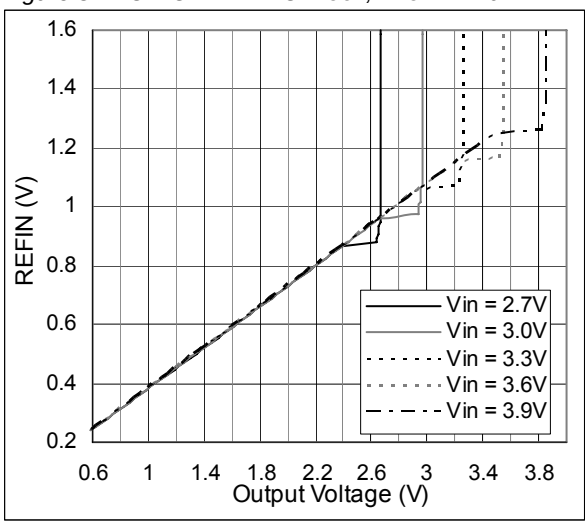


*Figure 9. DC-DC Efficiency vs. IOUT; VOUT = 0.8V*

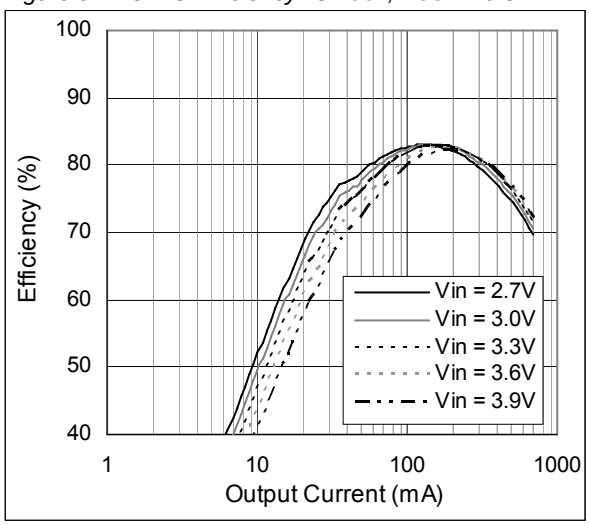



*Figure 10. DC-DC Efficiency vs. IOUT; VOUT = 1.2V*

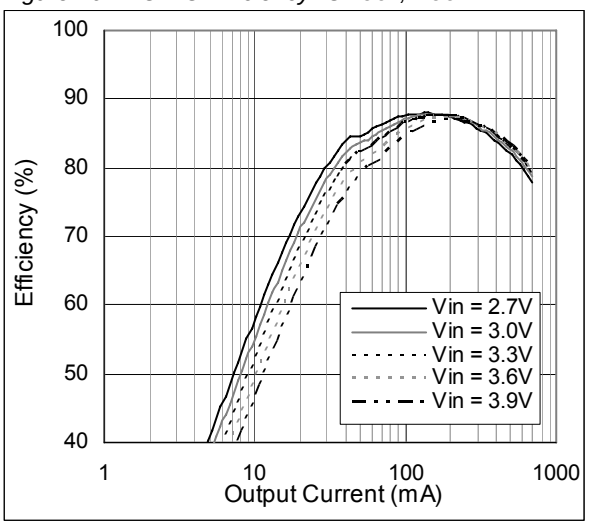



*Figure 11. DC-DC Efficiency vs. IOUT; VOUT = 1.8V*

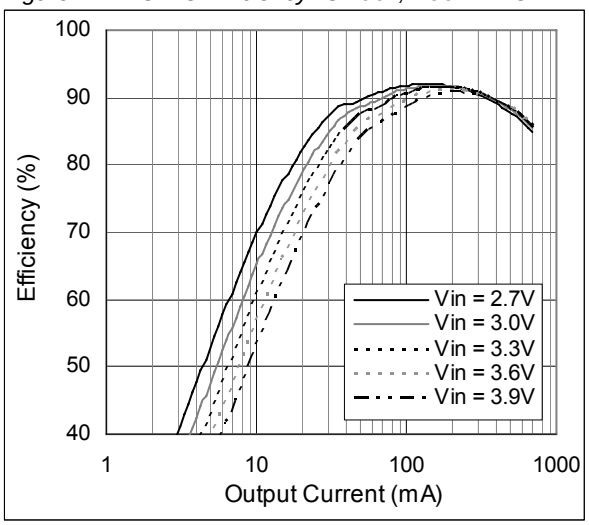



*Figure 12. DC-DC Efficiency vs. IOUT; VOUT = 2.2V*

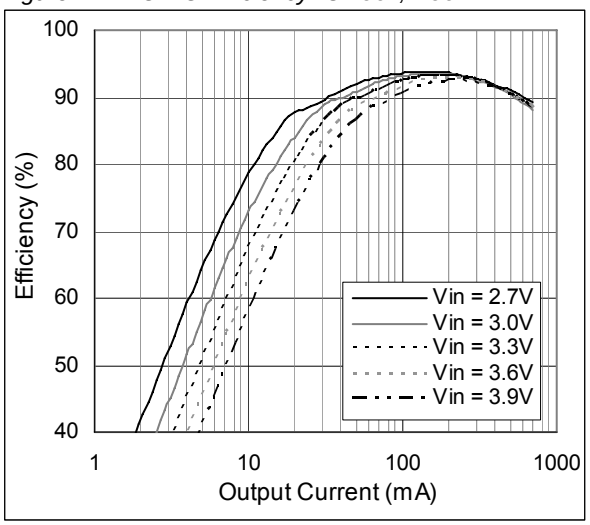



*Figure 13. DC-DC Load Regulation, VOUT vs. IOUT; VOUT = 0.8V*

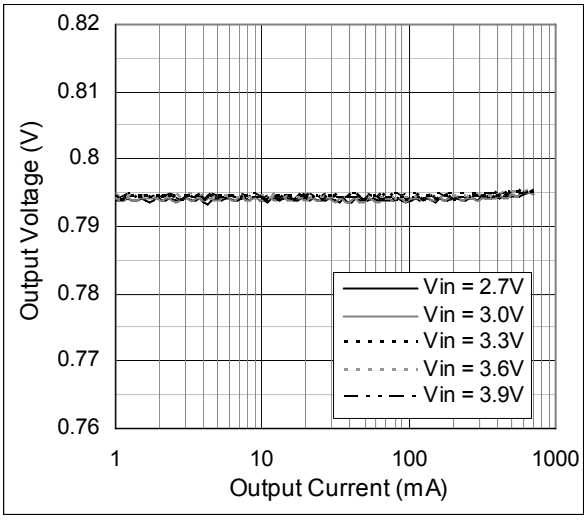



*Figure 14. DC-DC Load Regulation, VOUT vs. IOUT; VOUT = 1.2V*

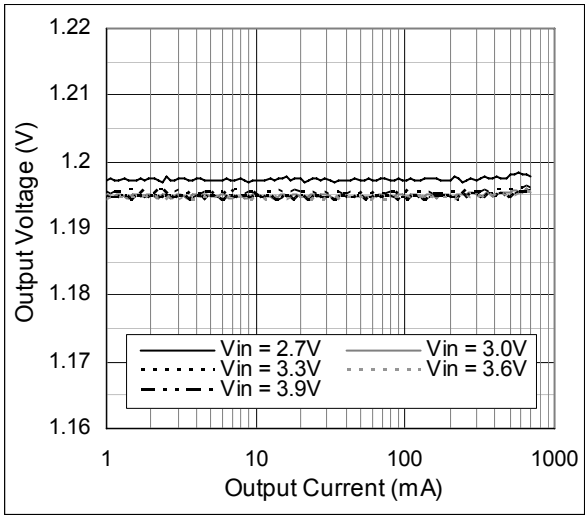


*Figure 15. DC-DC Load Regulation, VOUT vs. IOUT; VOUT = 1.8V*

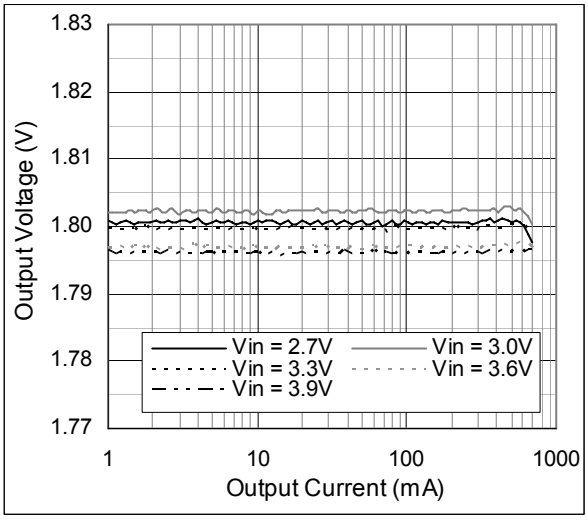



*Figure 16. DC-DC Load Regulation, VOUT vs. IOUT; VOUT = 2.2V*

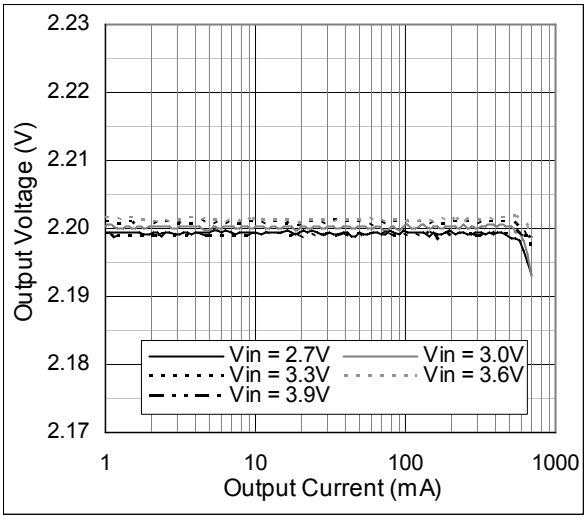



*Figure 17. DC-DC Efficiency vs VIN; VOUT = 3.8V*

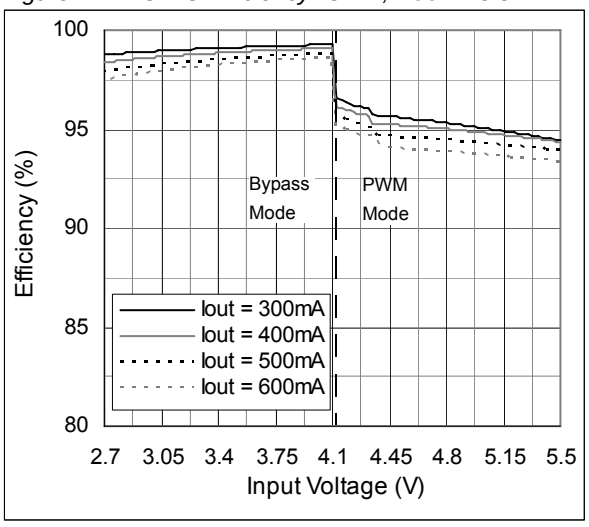



*Figure 18. DC-DC Efficiency vs VIN; VOUT = 3.4V*

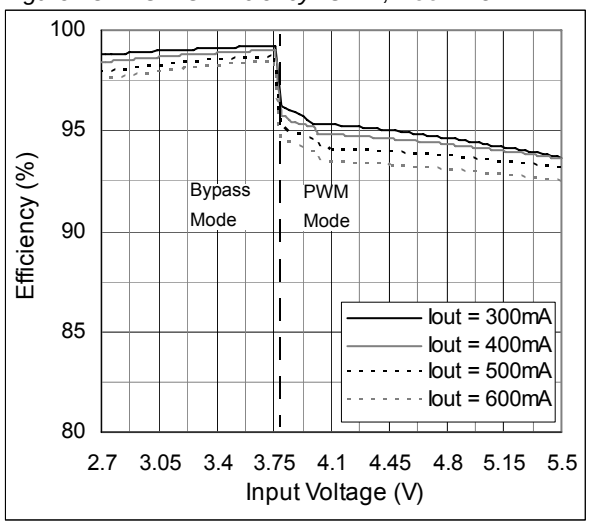



*Figure 19. DC-DC Efficiency vs VIN; VOUT = 2.0V*

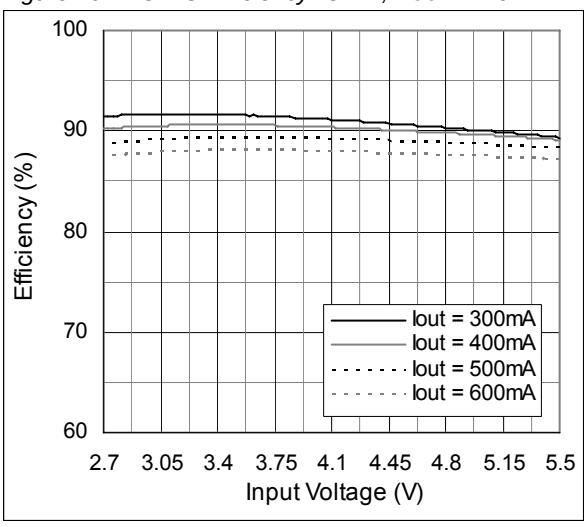



*Figure 20. DC-DC Efficiency vs VIN; VOUT = 1.5V*

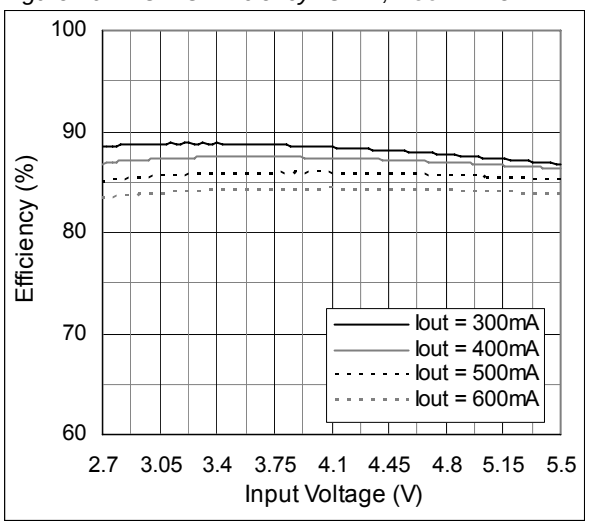


*Figure 21. DC-DC Efficiency vs Input Voltage; VOUT = 1.0V*

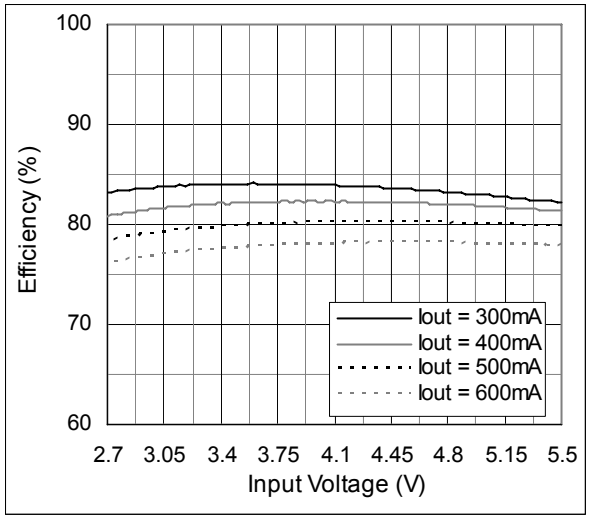



*Figure 22. DC-DC Line Regulation, VOUT vs. VIN; VOUT = 3.8V*

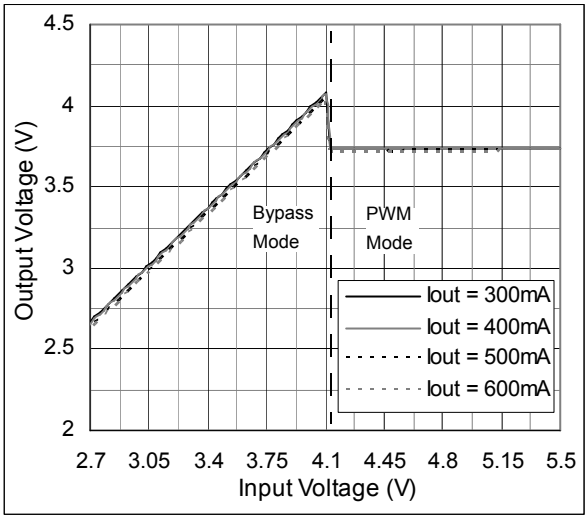



*Figure 23. DC-DC Line Regulation, VOUT vs. VIN; VOUT = 3.4V*

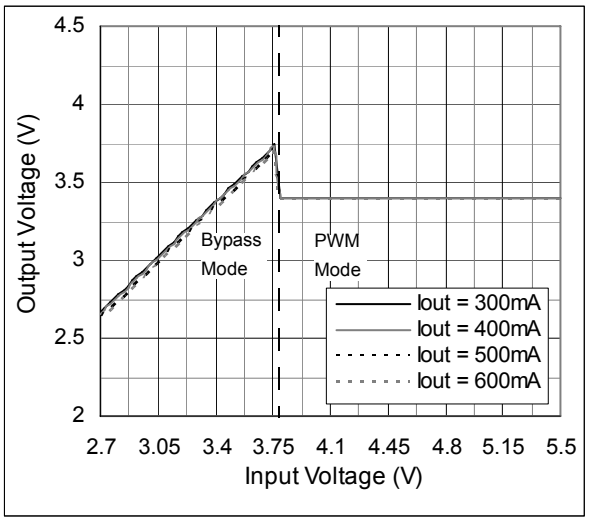



*Figure 24. DC-DC Line Regulation, VOUT vs. VIN; VOUT = 2.0V*

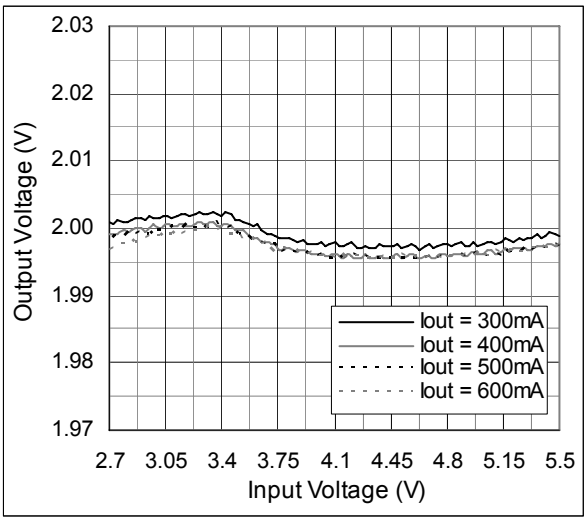



*Figure 25. DC-DC Line Regulation, VOUT vs. VIN; VOUT = 1.5V*

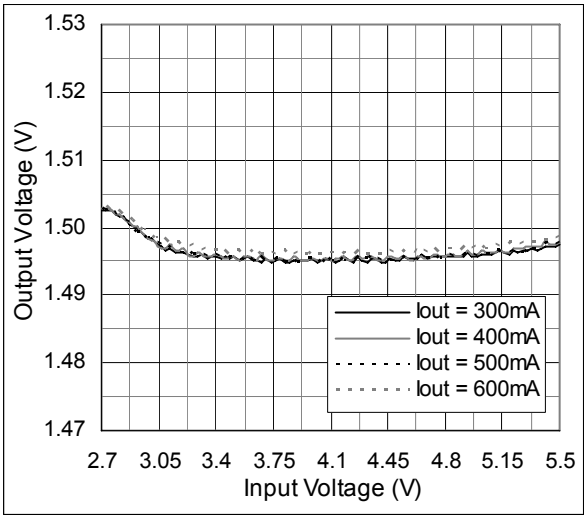



*Figure 26. DC-DC Line Regulation, VOUT vs. VIN; VOUT = 1.0V*

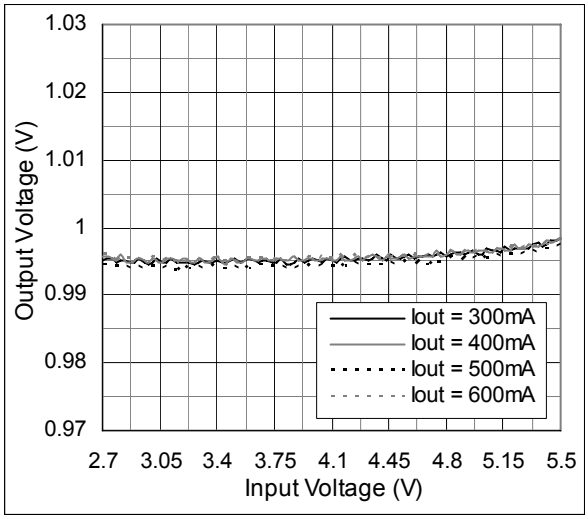


*Figure 27. DC-DC Output Voltage Error vs. Reference Voltage*

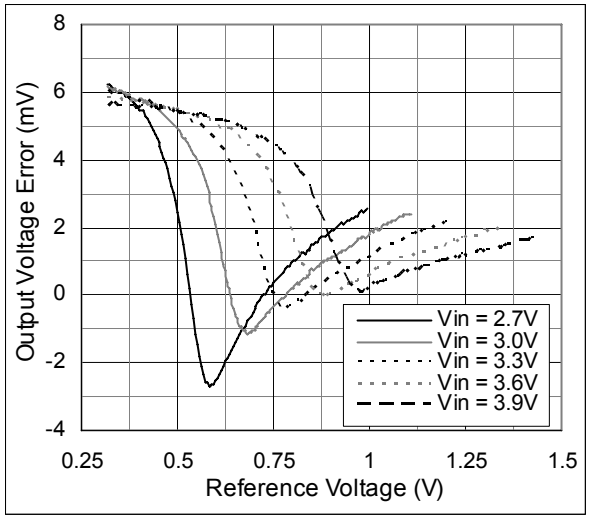



*Figure 28. DC-DC Bypass Dropout Voltage vs. Output Current*

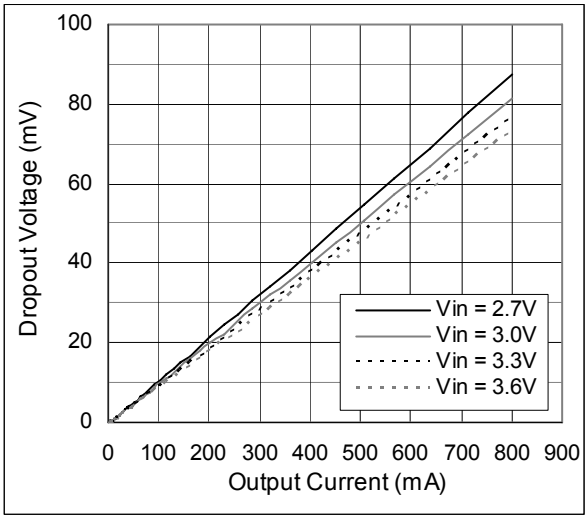



*Figure 29. DC-DC No-Load Supply Current vs. VIN*

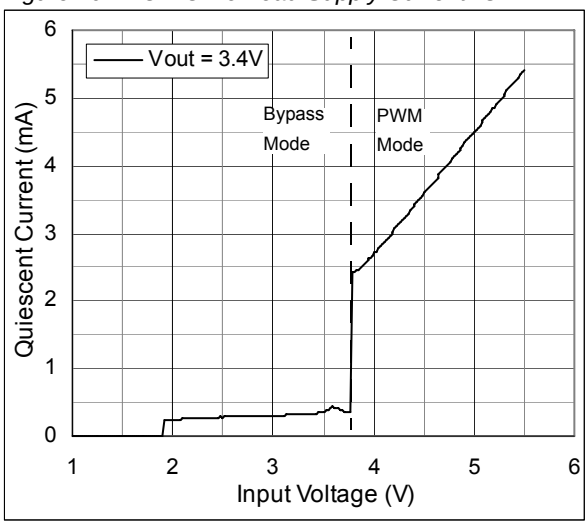



*Figure 30. Shutdown Supply Current vs. VIN*

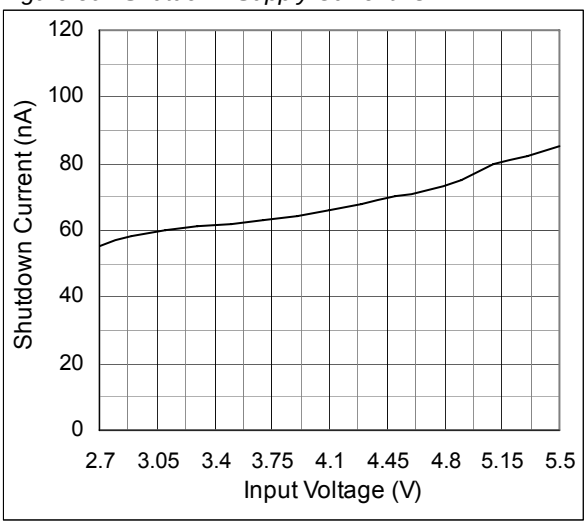



*Figure 31. DC-DC Switching; VIN=3.6V, VPA=1.2V, IOUT=50mA*

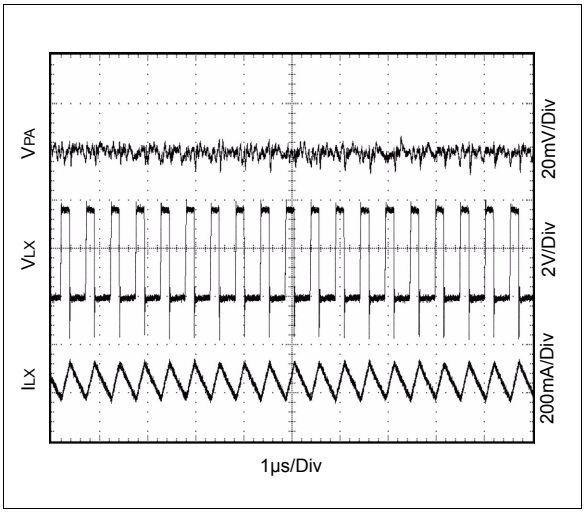



*Figure 32. DC-DC Switching; VIN=3.6V, VPA=1.2V, IOUT=500mA*

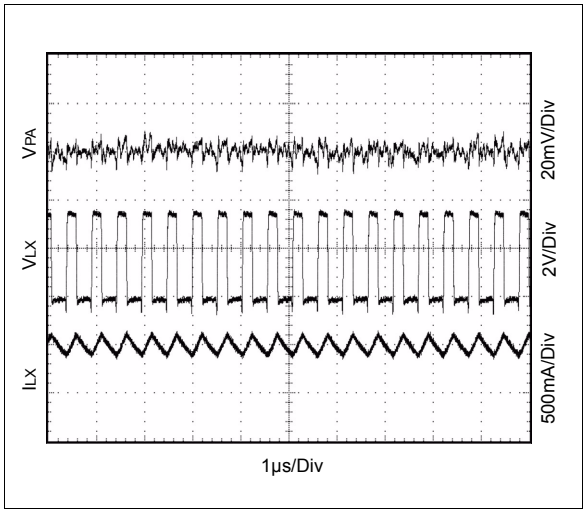


*Figure 33. DC-DC Soft-Start; $R_{LOAD}$ = 7.5Ω*

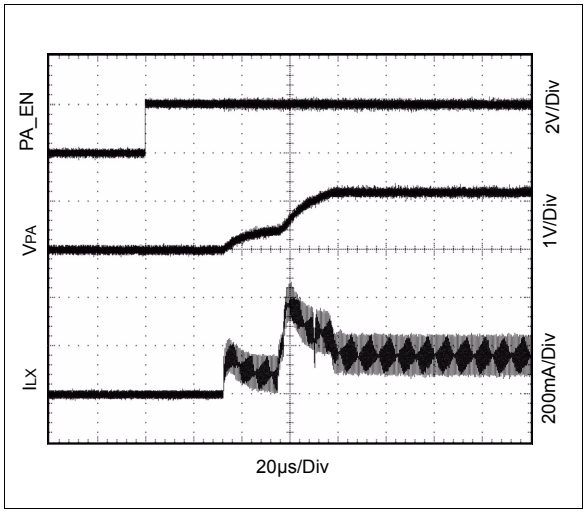



*Figure 34. DC-DC Shutdown*

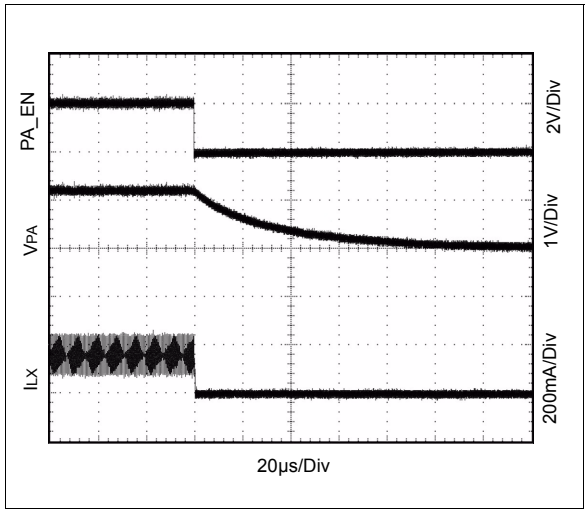



*Figure 35. DC-DC Sine Wave Output in PWM Mode; $V_{IN}$ = 4.5V, $R_{LOAD}$ = 7.5Ω*

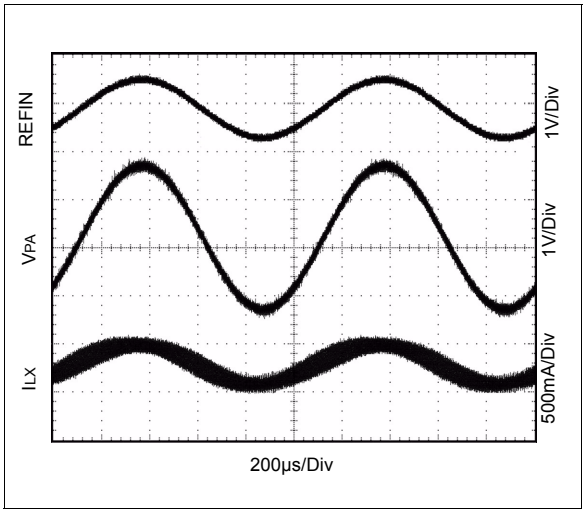



*Figure 36. DC-DC Sine Wave Output in Bypass Mode; $V_{IN}$ = 3.6V, $R_{LOAD}$ = 7.5Ω*

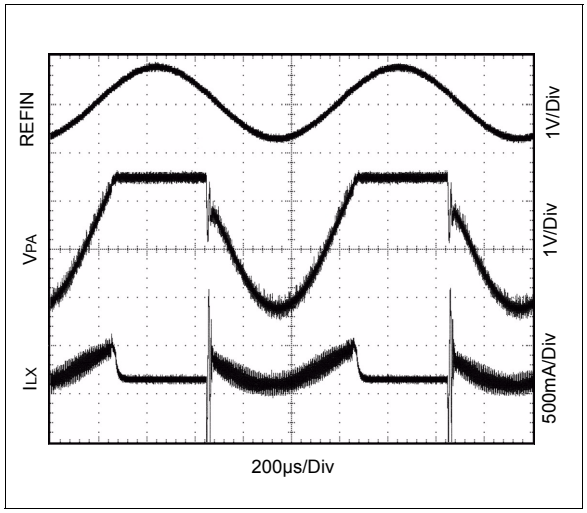



*Figure 37. DC-DC Rectangular Wave Output in PWM Mode; $V_{IN}$ = 4.5V, $R_{LOAD}$ = 7.5Ω*

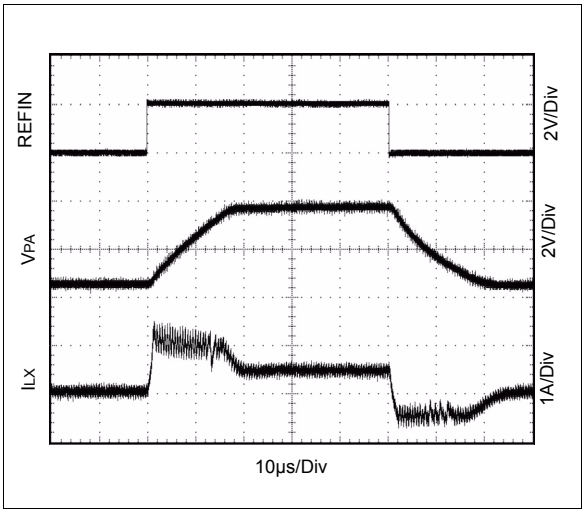



*Figure 38. DC-DC Rectangular Wave Output in Bypass Mode; $V_{IN}$ = 3.6V, $R_{LOAD}$ = 7.5Ω*

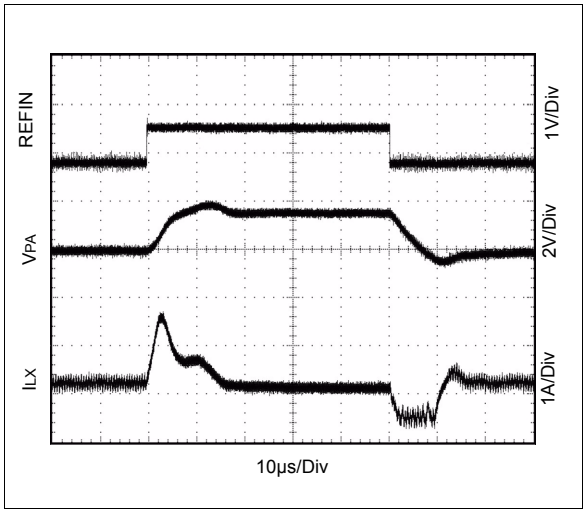


*Figure 39. DC-DC Line Transient; VIN = 4.0V to 3.5V, VOUT = 1.2V, RLOAD = 10Ω*

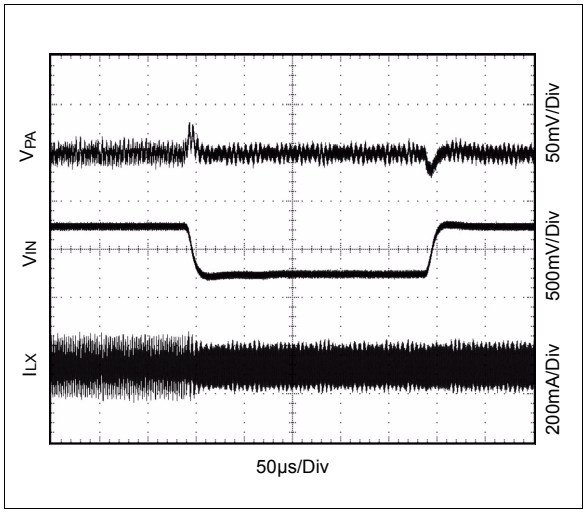



*Figure 40. DC-DC Load Transient; IOUT = 0mA to 500mA, VIN = 3.6V, VOUT = 2.5V*

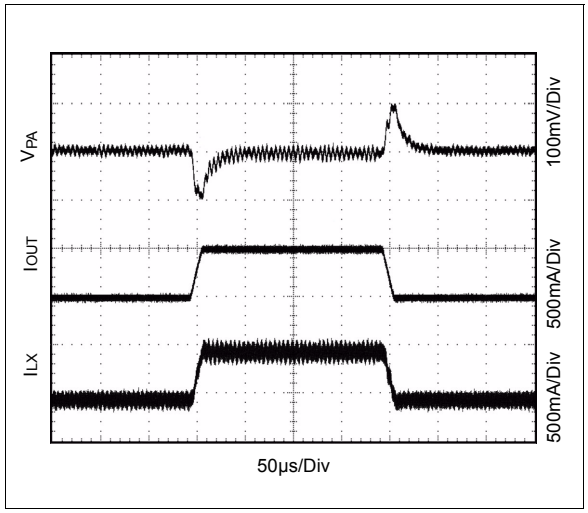



*Figure 41. LDO Quiescent Current vs. VIN*

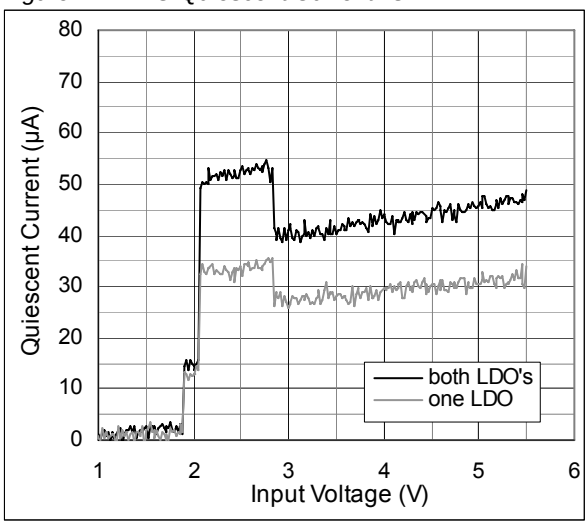



*Figure 42. LDO Line Regulation, VOUT vs. VIN*

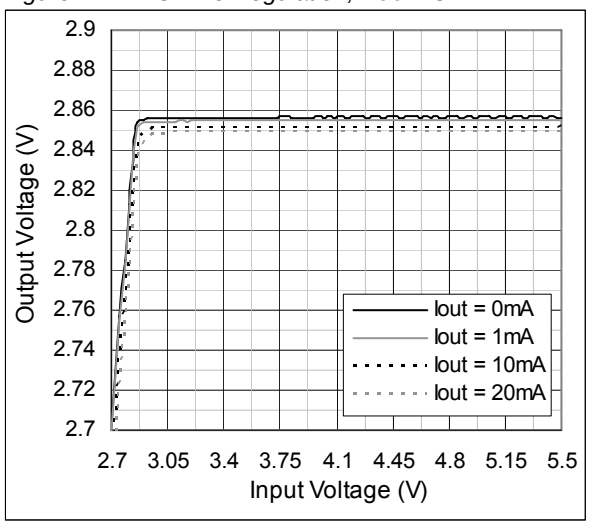



*Figure 43. LDO PSRR vs. Freq.; VIN = 3.2V, VOUT = 2.85V, VRIPPLE = 200mVPP, COUT =100nF*

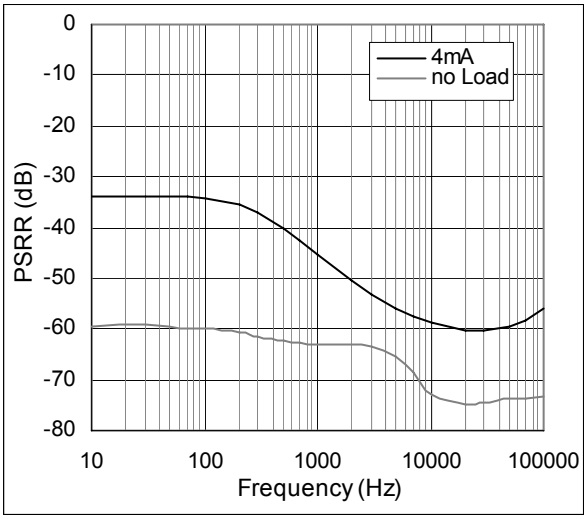



*Figure 44. LDO Output Noise vs. Freq.; VIN = 3.2V, VOUT = 2.85V, COUT =100nF*

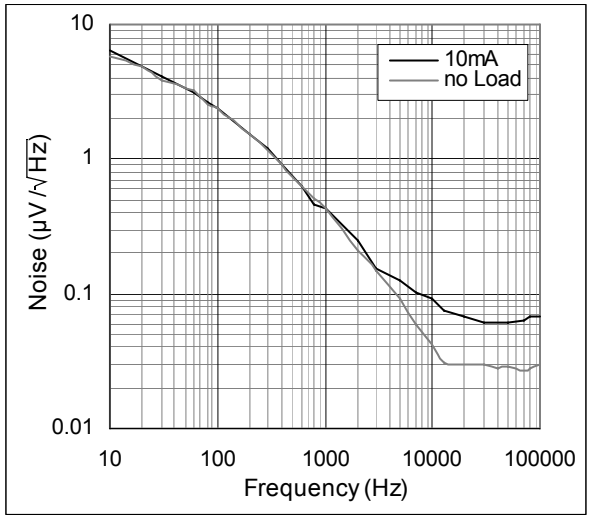


*Figure 45. LDO Turn ON / OFF Response; $V_{IN}$ = 3.6V, no load*

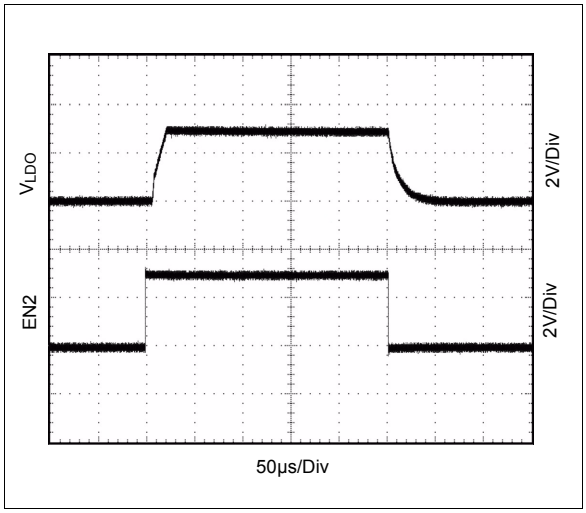



*Figure 46. LDO Load Transient; $I_{OUT}$ = 0mA to 10mA, $V_{IN}$ = 3.6V*

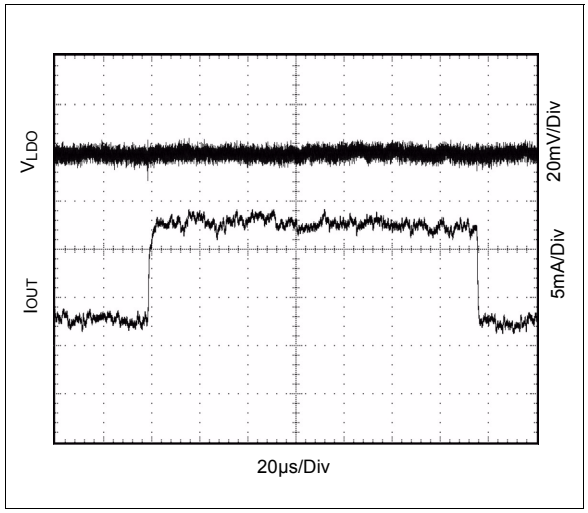



*Figure 47. LDO Line Transient; $V_{IN}$ = 5.5V to 3.5V, $I_{OUT}$ = 10mA*

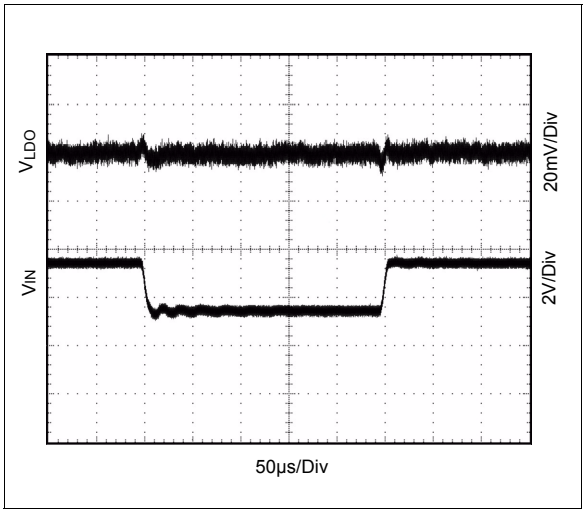
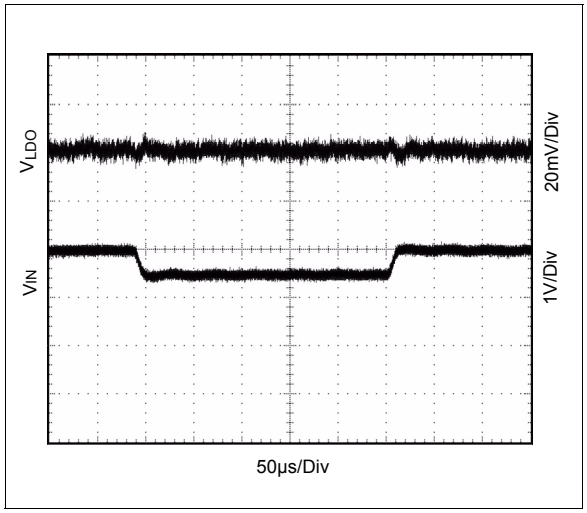


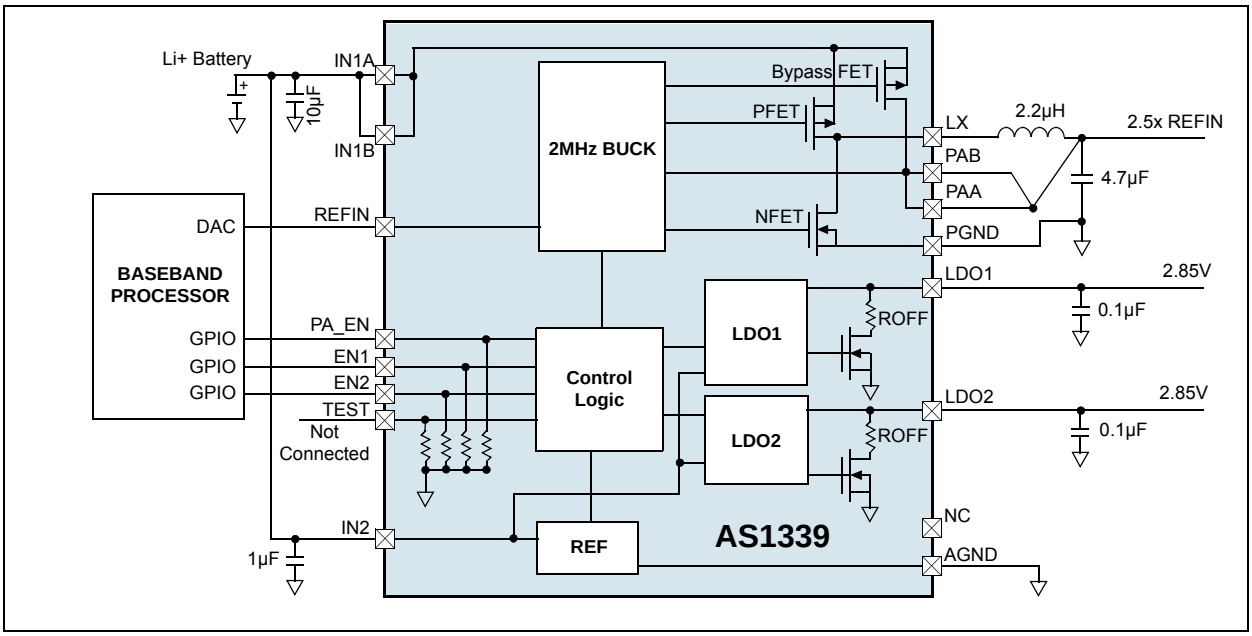

*Figure 48. LDO Line Transient; $V_{IN}$ = 4.0V to 3.5V, $I_{OUT}$ = 10mA*



# 8 Detailed Description

The AS1339 is designed to dynamically power the PA in WCDMA and NCDMA handsets. The device is empowered with a high-frequency, high-efficiency step-down converter, and two LDOs. The step-down converters are capable of delivering 650mA. The PWM control scheme provides fast transient response, while 2MHz switching frequency allows the trade-off between efficiency and small external components. A 110mΩ bypass FET connects the PA directly to the battery during high-power transmission.

*Figure 49. AS1339 - Block Diagram*




## Operating the AS1339

The AS1339's control block turns on the internal PFET (P-channel MOSFET) switch during the first part of each switching cycle, thus allowing current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (VIN - VOUT) / L, by storing energy in a magnetic field.

During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. As a result, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load.

While the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope of VOUT / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on-time to control the average current sent to the load.

The output voltage is equal to the average voltage at the LX pin.

While in operation, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control the power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle.

If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and

adjusts for the increase in the load. Before appearing at the PWM comparator, a slope compensation ramp from the oscillator is subtracted from the error signal for stability of the current feedback loop.

## Internal Synchronous Rectifier

To reduce the rectifier forward voltage drop and the associated power loss, the AS1339 uses an internal NFET as a synchronous rectifier. The big advantage of a synchronous rectification is the higher efficiency in a condition where the output voltage is low compared to the voltage drop across an ordinary rectifier diode. During the inductor current down slope in the second part of each cycle the synchronous rectifier is turned on. Before the next cycle the synchronous rectifier is turned off.

There is  no need for an external diode because the NFET is conducting through its intrinsic body diode during the transient intervals before it turns on.

## Bypass Mode

This mode connects IN1A and IN1B directly to PAA and PAB with the internal 110mΩ (typ) bypass FET, while the step-down converter is forced into 100% duty-cycle operation during high-power transmission. Due to the low on-resistance in this mode, the result is low dropout, high efficiency and a high output current capability.

The AS1339 enters bypass mode automatically when $V_{IN} \leq 2.69 \times V_{REFIN}$ and thus prevents excessive output ripple as the step-down converter approaches dropout. Due to an internal limitation of $V_{REFIN} \leq 1.5V$ the maximum output voltage is limited to 2.78 x 1.5V = 4.17V in Bypass Mode.

## Shutdown Mode

To put the PA step-down converter in shutdown mode, connect PA_EN to GND or disconnect PA_EN (NC =>logic-low). During shutdown mode, the control circuitry, internal switching MOSFET, and synchronous rectifier are turned off and LX becomes high impedance. For normal operation, connect PA_EN to IN1A/B or logic-high.

To place LDO1 or LDO2 in shutdown mode, connect EN1 or EN2 to GND or disconnect EN1 or EN2 (NC => logic-low). The outputs of the LDOs are pulled to ground through an internal 100Ω resistor during shutdown. When the PA step-down and LDOs are all in shutdown, the AS1339 enters a very low power state, where the input current drops to 0.8µA (typ).

**Note:** All enable Pins (PA_EN, EN1 and EN2) have an internal 110kΩ pull-down resistance.

## Soft-Start

The internal soft-start circuitry of the PA step-down converter limits inrush current at startup, reducing transients on the input source. Soft-start is favorable for supplies with high output impedance such as Li+ and alkaline cells. The DC-DC can start-up with full output load of 7.5Ω.

## Analog REFIN Control

The PA step-down converter uses REFIN to set the output voltage, which enables the converter to operate in applications requiring dynamic voltage control. The output voltage is limited to an upper level of 3.85V, when operating in PWM mode. In Bypass mode the output voltage is limited to $V_{IN}$.

**Notes:**

1. $V_{OUT} = 2.5 \times V_{REFIN}$
2. If REFIN is left floating the output voltage of the step-down converter can assume any value between 0.6V and $V_{IN}$.

## Thermal Overload Protection

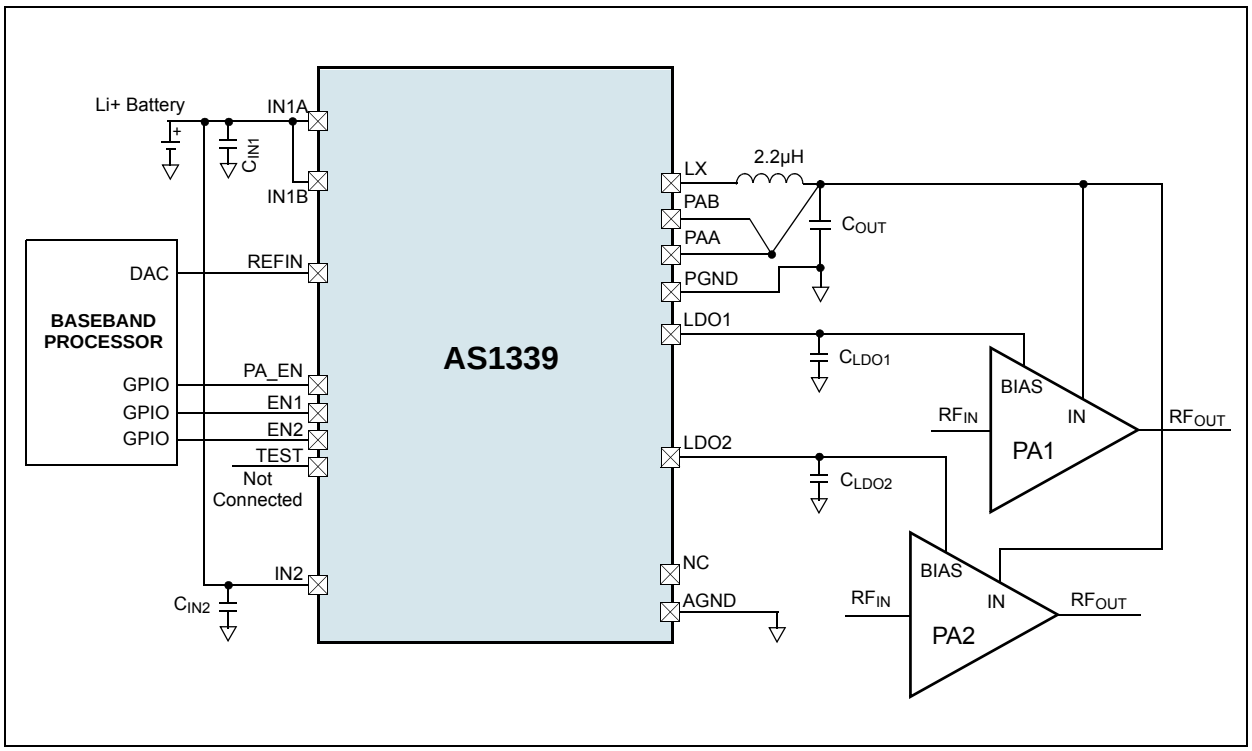
To prevent the AS1339 from short-term misuse and overload conditions the chip includes a thermal overload protection. To block the normal operation mode the device is turning off the PFET and the NFET in PWM and bypass mode as soon as the junction temperature exceeds 140°C. To resume the normal operation the temperature has to drop below 130°C.

**Note:** Continuing operation in thermal overload conditions may damage the device and is considered bad practice.

# 9 Application Information

The AS1339 is designed to supply power amplifiers for RF applications. The output power of the PA can directly be controlled via the output voltage of the AS1339. Figure 50 shows a typical application.

*Figure 50. Typical Application Diagram*




## Capacitor Selection for Step-Down Converter

### Input Capacitor

To reduce the current peaks drawn from the battery or power source and to reduce the switching noise in the device an input capacitor is highly recommended. At the switching frequency the impedance of the capacitor should be very low. It's recommended to use a X5R or X7R dielectric multilayer ceramic capacitor due to their small size, low ESR and small temperature coefficients. For most applications a 4.7µF capacitor is sufficient. To decrease the interfering noise and to lower the input ripple the capacitor value can be set higher (e.g. 10µF).

### Output Capacitor

To ensure a stable loop regulation and a small output voltage ripple a low impedance capacitor should be used. It's recommended to use a X5R or X7R dielectric multilayer ceramic capacitor due to their small size, low ESR and small temperature coefficients. For most applications a 4.7µF capacitor is sufficient. To achieve a better load-transient performance and to decrease the output ripple the capacitor value can be set higher (e.g. 10µF).

*Table 6. Recommended Capacitors for the Step-Down Converter*

| Name | Part Number | C | Voltage | Type | Size | Manufacturer |
|---|---|---|---|---|---|---|
| $C_{IN1}$, $C_{OUT}$ | GRM21BR60J106KE01 | 10µF | 6.3V | X5R | 0805 | Murata www.murata.com |
| | GRM21BR61C475KA88 | 4.7µF | 16V | X5R | 0805 | |
| | C0603C475K8PAC7867 | 4.7µF | 10V | X5R | 0603 | KEMET www.kemet.com |

## Capacitor Selection for LDO's

### Input Capacitor

The capacitor for the LDO Input should have at least a value of the sum of the output capacitors of LDO1 and LDO2. With a larger input capacitance and lower ESR a better noise rejection and line transient response can be achieved.

### Output Capacitor

For the LDO outputs the capacitor value depends on the needed load current. For a stable operation with rated maximum load currents a minimum output capacitor of 1µF is recommended. At light loads of 10mA or less a 0.1µF capacitor is sufficient. With larger output capacitance a reduced output noise, improved load-transient response, better stability and power-supply rejection can be achieved.

*Table 7. Recommended Capacitors for the LDO's*

| Name | Part Number | C | Voltage | Type | Size | Manufacturer |
|---|---|---|---|---|---|---|
| $C_{IN2}$, $C_{LDO1}$, $C_{LDO2}$ | C0402C104K4RAC | 100nF | 16V | X7R | 0402 | KEMET www.kemet.com |
| | GRM155R61A105KE15 | 1µF | 10V | X5R | 0402 | Murata www.murata.com |

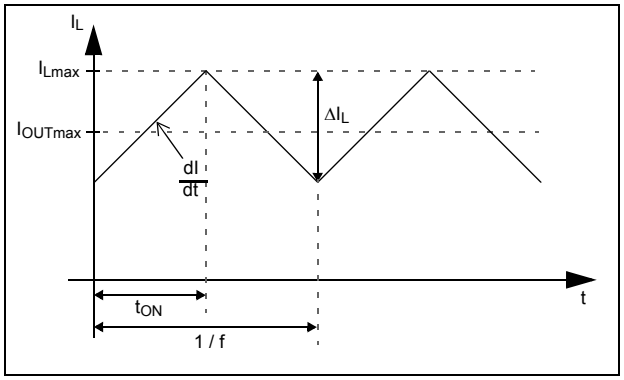
## Inductor Selection

For most applications the value of the external inductor should be in the range of 1.5µH to 4.7µH as the inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current ($\Delta I_L$) decreases with higher inductance and increases with higher $V_{IN}$ to $V_{OUT}$.

In Equation (EQ 3) the maximum inductor current in PWM mode under static load conditions is calculated. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation (EQ 4). This is recommended because the inductor current will rise above the calculated value during heavy load transients.

The inductor current ripple $\Delta I_L$ (see EQ 3) is defined by the slope of the current (dI / dt) (see EQ 1) multiplied by the PFET on-time $t_{ON}$ (see EQ 2).

*Figure 51. Ripple Current Diagram*




$$\frac{dI}{dt} = \frac{V_{IN} - V_{OUT}}{L} \qquad \textit{(EQ 1)}$$

$$t_{ON} = DutyCycle \times \frac{1}{f} \qquad DutyCycle = \frac{V_{OUT}}{V_{IN}} \qquad \textit{(EQ 2)}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f \times L} \quad \textit{(EQ 3)}$$

$$I_{LMAX} = I_{OUTMAX} + \frac{\Delta I_L}{2} \quad \textit{(EQ 4)}$$

f .... Switching Frequency (2.0MHz typical)
L .... Inductor Value
$I_{LMAX}$ .... Maximum Inductor current
$\Delta I_L$ .... Peak to Peak inductor ripple current
$I_{OUTMAX}$ .... Applied load current

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability. The total losses of the coil have a strong impact on the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance and the following frequency-dependent components:

1. The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
2. Additional losses in the conductor from the skin effect (current displacement at high frequencies)
3. Magnetic field losses of the neighboring windings (proximity effect)
4. Radiation losses

**Note:** For highest efficiency, a low DC-resistance inductor is recommended.

*Table 8. Recommended Inductors*

| Part Number | L | DCR | Current Rating | Dimensions (L/W/T) | Manufacturer |
|---|---|---|---|---|---|
| MLP2520S1R5S | 1.5µH | 80mΩ | 1.5A | 2.5x2.0x1.2mm | TDK www.tdk.com |
| MLP2520S2R2S | 2.2µH | 110mΩ | 1.2A | 2.5x2.0x1.2mm | |
| MLP2520S3R3S | 3.3µH | 110mΩ | 1.0A | 2.5x2.0x1.2mm | |
| EPL2014-222MLC | 2.2µH | 120mΩ | 0.98A | 2.2x2.0x1.4mm | Coilcraft www.coilcraft.com |
| EPL2014-332MLC | 3.3µH | 152mΩ | 0.8A | 2.2x2.0x1.4mm | |
| EPL2014-472MLC | 4.7µH | 231mΩ | 0.65A | 2.2x2.0x1.4mm | |
| XPL2010-222ML | 2.2µH | 156mΩ | 1.2A | 2.0x1.9x1.0mm | |
| XPL2010-332ML | 3.3µH | 207mΩ | 0.925A | 2.0x1.9x1.0mm | |

*Figure 52. Efficiency Comparison of different Inductors; VIN = 3.9V, VOUT = 1.0V*

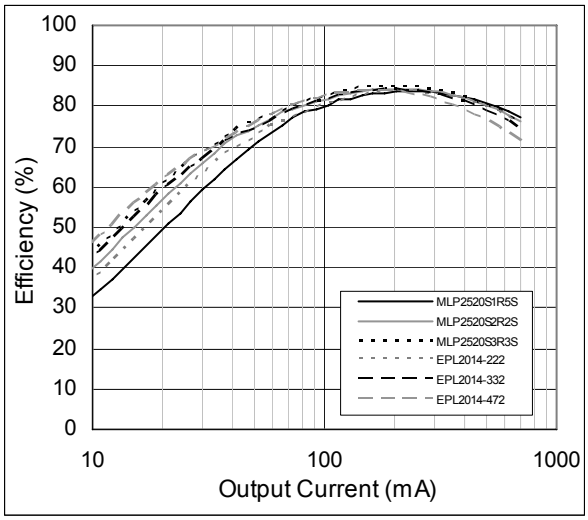
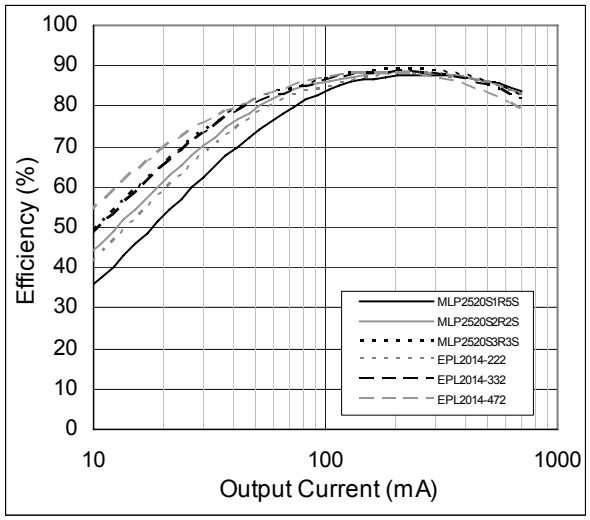



*Figure 53. Efficiency Comparison of different Inductors; VIN = 3.9V, VOUT = 1.5V*




## Example

The following system should be designed:

- A supply with a Lithium-Ion Battery = 4.5V
- VOUT = 3.0V
- IOUTMAX = 500mA

For the first step VREF is calculated as shown in Equation (EQ 5).

$$V_{REF} = \frac{V_{OUT}}{2,5} = 1,2V \quad \textit{(EQ 5)}$$

$$V_{IN} \leq 2,69 \times V_{REF} \quad \textit{(EQ 6)}$$

Due to Equation (EQ 6): VIN = 3.23V

If VIN is falling below 3.23V the device is going into Bypass mode (see Bypass Mode on page 17).

Hence a 2.2µH coil is used, ΔIL can be calculated with Equation (EQ 3): ΔIL= 227mA

With this result IMAX can be calculated with Equation (EQ 4): IMAX = 614mA.

The saturation current of the coil should be chosen slightly higher than IMAX because heavy load transients could increase the peak current. For a short period of time (~50µs) the peak inductor current can rise up to a value of approximately 1.1A (p-channel MOSFET peak current limit). In this case a coil with a rated saturation current of ~800mA can be chosen.

## Layout Considerations

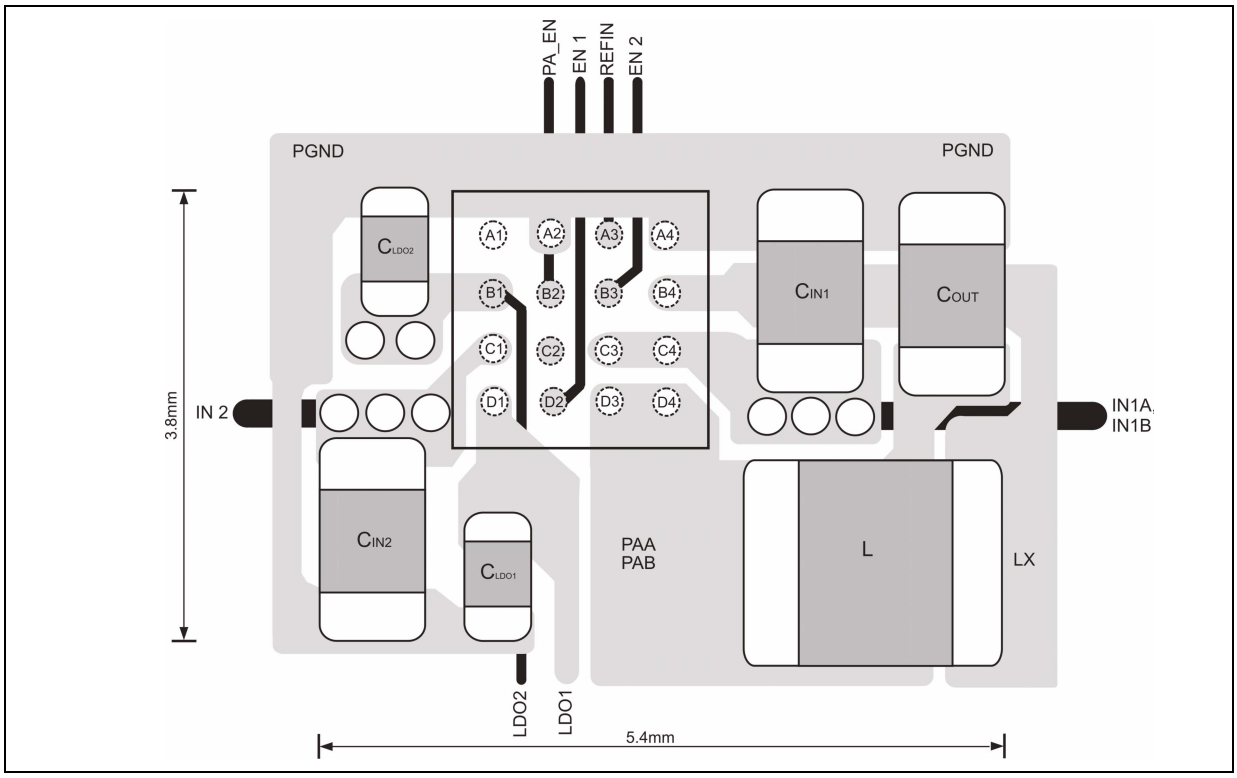
Please carefully observe that large peak currents of up to 1.1A and high switching frequencies will make the PCB layout a very important part of the system performance and compliance. A proper PCB design will minimize electro magnetic interference (EMI) as well as voltage gradients in the ground plane, which both can result in application instabilities. Please closely follow the guidelines as mentioned below.

- Keep the power traces as short and wide as possible (IN1A, IN1B, IN2, LX, PAA, PAB, PGND)
- Place all capacitors as close as possible to the pins of the device
- Avoid voltage gradients in the ground plane

Please note the following PCB layout considerations shown in Figure 54:

- The negative terminals of COUT and CIN1/CIN2 are kept as close as possible to each other. It is recommended to connect these terminals directly to PGND at a star point.
- The current path between pins IN1A/IN1B (C3/C4) and pin PGND (A4) via CIN1 is routed very short
- The current path between pins PAB/PAA (D3/D4) and pin PGND (A4) via COUT is routed very short
- The connection between LX (B4) and pins PAB/PAA (D3/D4) via the coil (L) is routed very short
- To keep the cross-coupling between the LDOs and DC/DC minimized, in regard to supply ripple and noise induction, the IN1 and IN2 path are separated. Both power inputs should be connected at a star point directly at the main supply
- To prevent voltage gradients between AGND (A2) and PGND (A4), these pins are connected via a short, low ohmic, trace to each other.

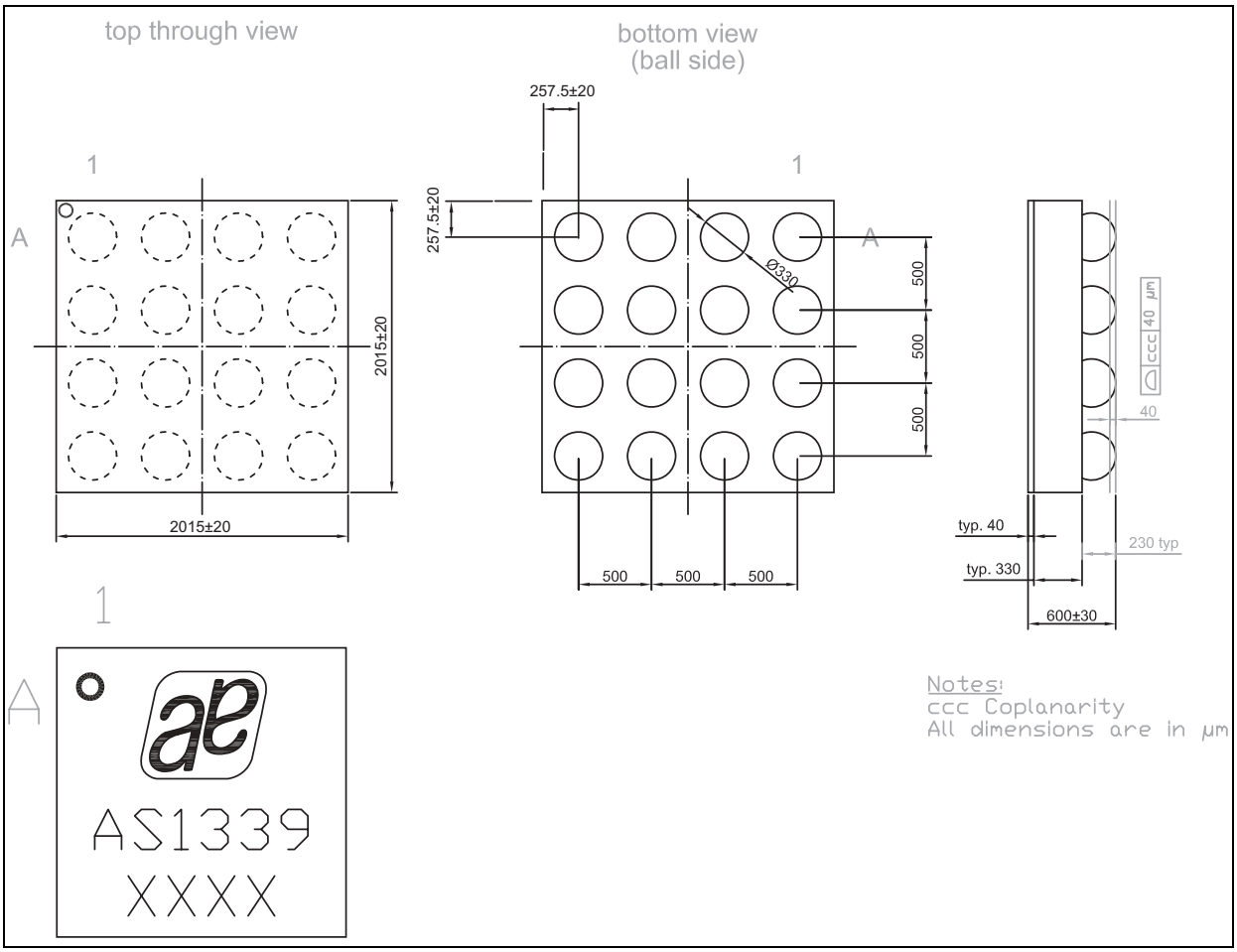
*Figure 54. Layout for Space Limited Applications*



# 10 Package Drawings and Markings

The devices are available in a 16-pin WLP (2x2mm) package.

*Figure 55. 16-pin WLP (2x2mm) Package*



# 11 Ordering Information

The devices are available as the standard products shown in Table 9.

*Table 9. Ordering Information*

| Ordering Code | Marking | Description | Delivery Form | Package |
|---|---|---|---|---|
| AS1339-BWLT | AS1339 | 650mA RF Step-Down DC-DC for PA, with two LDOs | Tape and Reel | 16-pin WLP (2x2mm) |

**Note:** All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
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