

PCN #: 08_0105

Title:

ADF4156 Redesign : Improve Phase Noise performance when using reference doubler and reduce power down current.

Date Published:

October 22, 2008

Type:

Device

Part Number:

ADF4156

Proposed Change:

1) Tie unused PFD/CP blocks power supplies to GND to reduce power down current from 4mA to <10uA.

2) Invert reference clock path from the output of reference doubler to reduce phase noise when Reference Doubler is enabled resulting in 10-12dBc/Hz In Band phase noise improvement.

These changes will have no effect on the part in normal operation if the doubler is not being used.

This change will have no effect on the form, fit, function, quality or reliability of the device other than doubler operation as outlined above.

Samples of the changed product are available now.

Reason for Change:

1) To reduce power-down current to <10uA

2) To allow reference doubler operation without phase noise degradation (Current silicon exhibits a 6dBc/Hz phase noise degradation when doubler is enabled).

This change is only relevant where the reference double operation is used.

Summary of Supporting Information:

Edits were verified in bench characterization.

Planned Date Change Effective:

October 22, 2008

EIA Date Code:

0850

Contact:

Peadar Forbes

Application Engineer

Phone: 353 61 495745

Fax: 353 61 304094

Email: peadar.forbes@analog.com

Analog Devices, Inc.

