Spartan-3A XC3S700A Errata for Engineering Samples

Introduction

Thank you for your interest in the Xilinx XC3S700A FPGA device engineering samples. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in this errata notification.

Device Identification

These errata apply to the XC3S700A engineering samples as shown in Table 1. See the top-mark in Figure 1.

Table 1: **XC3S700A Devices Affected by These Errata**

Device Types	XC3S700A
Packages	All
Speed Grades	-4C
Date Codes	All
Marked as "ES"	Yes

Traceability

XC3S700A engineering samples are marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

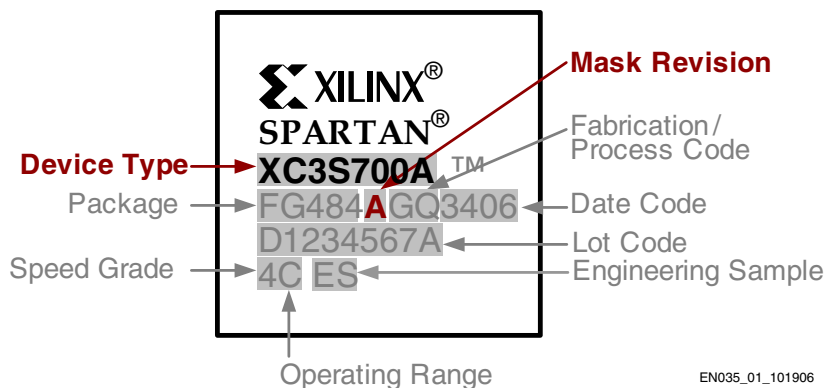

Figure 1: **XC3S700A FPGA Top Marking**

Hardware Errata Summary

Table 2 summarizes the known hardware issues with the XC3S700A engineering samples. See Hardware Errata for a detailed description of each known issue. Table 2 also shows which mask revision is affected by a particular errata item.

Table 2: **Hardware Errata Summary**

Errata Issue	Severity	Engineering Samples	Production Devices
"PCI Clamp Diode Unavailable"	Minor	Applies	Does Not Apply
"DCM Digital Frequency Synthesizer Requires Additional Lock Circuitry"	Minor	Applies	Fixed in ISE^{TM} 9.1i software
"Potential Data Slip Issue with ODDR2 Output Flip-Flop Using C0 Alignment"	Minor	Applies	Does Not Apply
"Block RAM Readback Feature Unavailable"	Minor	Applies	Does Not Apply

Hardware Errata

This section provides a detailed description of each known hardware issue.

PCI Clamp Diode Unavailable

Applications affected

This issue only affects PCI bus and card applications that require full compliance to the PCI bus standard. It has little to no effect on point-to-point PCI solutions, such as chip-to-chip communication on the same board. The XC3S700A engineering samples are still useful for PCI bus card development but must not be used for PCI bus production designs.

Description

The PCI clamp diode shunts the potentially large overshoot voltage possibly generated in a PCI bus plug-in card application, which protects the FPGA I/O circuitry. The PCI clamp diode feature is not available on the XC3S700A engineering samples.

Workaround

None. This issue has been corrected in production revisions of the XC3S700A silicon.

DCM Digital Frequency Synthesizer Requires Additional Lock Circuitry

Applications affected

This issue potentially affects only those applications that use the Digital Frequency Synthesizer (DFS)—which is part of the Digital Clock Manager (DCM).

Description

A small number of DCM DFS locking failures have been observed during characterization.

Workaround

A software workaround exists, as shown in Figure 2. This circuit is automatically inserted by the ISE development software starting with version 9.1i. Using FPGA logic, the circuit monitors both the LOCKED output from the DCM_SP function and the STATUS[2] bit, which indicates that the DFS output CLKFX has stopped. If LOCKED = 0 and STATUS[2] = 1, then the circuit asserts the DCM RESET input. If the FPGA application also resets the DCM, then OR the reset signal from the FPGA application with the monitored output signals.
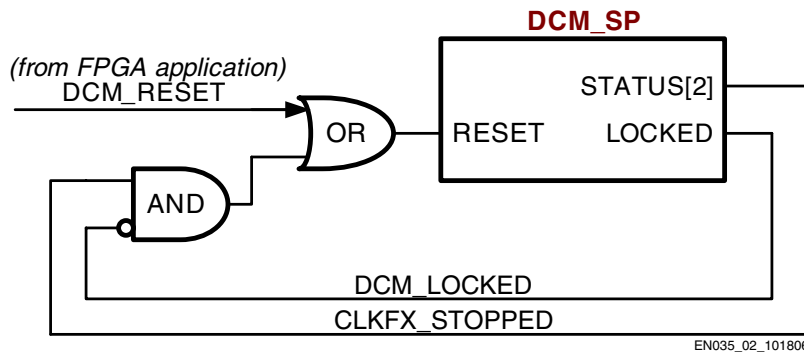
Figure 2: **DCM DFS Lock Failure Workaround**

Potential Data Slip Issue with ODDR2 Output Flip-Flop Using C0 Alignment

Applications affected

The ODDR2 output flip-flop primitive is typically used in high-speed differential I/O applications, such as LVDS and RSDS interfaces. This only affects applications using DDR_ALIGNMENT=C0 or C1. The default ODDR2 flip-flop without the alignment feature remains fully supported, and the IDDR2 alignment feature is supported.

Description

Data slip has been observed under certain BUFG placement situations for engineering samples.

Workaround

It is possible to use an alternate implementation inside the FPGA fabric using logic slice functions and careful placement between the slice flip-flop and adjacent I/O block. For details, see Answer 24478. This issue has been corrected in production revisions of the XC3S700A silicon.

Block RAM Readback Feature Unavailable

Applications affected

This issue only affects the rare application that might use the Readback feature to read block RAM contents.

Description

Reading back block RAM contents is not available in engineering samples. This issue does not affect the iMPACT Verify operation or ChipScope™ operations.

Workaround

None. This issue has been corrected in production revisions of the XC3S700A silicon.

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications. For questions about these errata, please contact Xilinx Technical Support http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx sales representative, http://www.xilinx.com/company/contact.htm.

Obtaining Errata Notification Updates

If this document is printed or saved locally, please check for the most recent release, available to registered users on the Xilinx web site at http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata. To receive an e-mail alert when this document changes, sign up at http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

Applicable Documents

These errata apply to the following XC3S700A documents:

- **DS529: Spartan™-3A FPGA Family Data Sheet**
  www.xilinx.com/bvdocs/publications/ds529.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/bvdocs/userguides/ug331.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Description
12/01/06	1.0	Initial release
04/16/07	1.1	Updated to note that all errata are fixed in production silicon.