PCN Number:		20160117003				PCN Da	te:	1/18/2016	
Tit	le:	Datasheet for	DAC3482						
			PCN Manager	PCN Manager			pt:	Qua	lity Services
Ch	ange	Type:		•					,
		ssembly Site		\square	Design		Wafer	Bum	n Site
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10/	(u5 II)			nou	neing an mormation only i	locin			
The	e proc	luct datasheet(s)	is being upo	late	d as summarized below.				
The following change history provides further details.									
	in Tr	VAC							
	Υ IE IN	XAS STRUMENTS						D	AC3482
- 1					SLAS748F -	-MARC	H 2011-RE	/ISED AU	GUST 2015
С	hanges	from Revision E (Feb	ruary 2013) to R	evisi	on F				Page
•					tion, Device Functional Modes, Applic				
	section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section								
•		· · ·							
•					pin if SLEEP pin is set to logic HIGH				
•	Added additional circuit configuration for unused terminals						11		
•	Changed DAC3484 to DAC3482 in SDENB description 11						11		
•	Adde	d additional operation re	quirement for SL	EEP	pin if SLEEP pin is set to logic HIGH	befor	e and duri	ng devi	ce
•					vel to Single-Ended Input Level to bet				
			-	-	vel.				
•	Added DACCLK and OSTR minimum voltage note to Electrical Characteristics – Digital Specifications								
•	Added text and application report link to Input FIFO section								
•	Added reference to LMK0480x family in Input FIFO section								
•	Added pin number per package for LPF pin in PLL Mode section								
•	Changed figure and table references in FIR Filters section								
•	Changed first paragraph in Complex Signal Mixer section								
•	Deleted redundant text from Related Documentation section								
Changed point to pointer in DAC3482 Alarm Monitoring section									
•	-				ring section				
•	Added	note to Figure 80							52
•	Added	I V _{COM} values to Table 9							53
		led Unused LVDS Port Termination section							

•	Added clarification on timing requirement acronyms to Sources Mode.			50		
•	Deleted or in Power-Up Sequence description					
•	Changed P = 3 to P = 4 in PLL Configuration to reflect the correct example start-up routine configuration					
•	Added pin description for both packages					
•	Changed Config7, bit 3 naming typo					
•	Changed config10 to config11 and 0x0A to 0x0B in register config11					
•	Changed QMC offset registers to QMC correction registers in config16 function					
•	Changed Qfine to fine in config18 function					
•	Added reference in config26 function					
•	Added additional operation requirement for SLEEP pin power up and initialization in config27 function			76		
•	Changed 1.2VDIG to DIGVDD in config27 function					
•	Added pin description for both packages to register cor	nfig35 description		79		
•	Added reference to Digital Input Timing Specifications in register config36 description					

These changes may be reviewed at the datasheet links provided. http://www.ti.com/product/DAC3482

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:				
DAC3482IRKD25	DAC3482IRKDR	DAC3482IRKDT	DAC3482IZAY	DAC3482IZAYR

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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