Linear RF Power FET
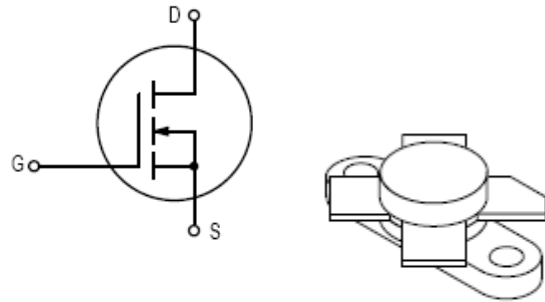# 30 W, 175 MHz, 50 V

MACOM®

Features

- Superior High Order IMD
  IMD(d3) (30 W PEP): -35 dB
  IMD(d11) (30 W PEP): -60 dB
- Specified 50 V, 30 MHz Characteristics:
  Output Power: 30 W
  Gain: 18 dB
  Efficiency: 40%
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Lower Reverse Transfer Capacitance: 3 pF

Applications

- Industrial, Commercial & Amateur Radio Equipment to 175 MHz.

Description

The MRF148B is a linear RF Power FET designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175 MHz.

CASE 211–07, STYLE 2

Electrical Specifications: T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Off Characteristics					
Drain Source Breakdown Voltage	V_{GS} = 0, I_D = 10 mA	Vdc	120	—	—
Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0	mAdc	—	—	1
Gate Body Leakage Current	V_{GS} = 20 V, V_{DS} = 0	nAdc	—	—	100
On Characteristics					
Gate Threshold Voltage	V_{DS} = 10 V, I_D = 10 mA	Vdc	0.8	2.5	5.0
Drain Source On-Voltage	V_{GS} = 10 V, I_D = 2.5 A	Vdc	1.0	3.0	5.0
Forward Transconductance	V_{DS} = 10 V, I_D = 2.5 A	Mhos	0.8	1.2	—
Dynamic Characteristics					
Input Capacitance	V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz	pF	—	62	—
Output Capacitance	V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz	pF	—	35	—
Reverse Transfer Capacitance	V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz	pF	—	3	—

For further information and support please visit:
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Parameter	Test Conditions	Units	Min.	Typ.	Max.
Functional Tests (SSB)					
Common Source Amplifier Power Gain	V_{DD} = 50 V, P_{OUT} = 30 W (PEP), I_{DQ} = 100 mA 30 MHz 175 MHz	dB	—	18 15	—
Drain Efficiency	V_{DD} = 50 V, f = 30 MHz, I_{DQ} = 100 mA 30 W PEP 30 W CW	%	—	40 50	—
Intermodulation Distortion	V_{DD} = 50 V, P_{OUT} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA	dB	—	-35 -60	—
Load Mismatch	V_{DD} = 50 V, P_{OUT} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all phase angles	No Degradation in Output Power			
Class A Performance					
Power Gain	V_{DD} = 50 V, P_{OUT} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1 A	dB	—	20	—
Intermodulation Distortion[1]	V_{DD} = 50 V, P_{OUT} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1 A	dB	—	-50 -70	—

1. To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

Absolute Maximum Ratings[5,6]

| Parameter	Absolute Maximum
Drain-Source Voltage	120 Vdc
Drain-Gate Voltage	120 Vdc
Gate-Source Voltage	±40 Vdc
Drain Current—Continuous	6 Adc
Total Device Dissipation @ T_C = 25°C. Derate above 25°C	115 W
Junction Temperature	+200°C
Storage Temperature	-65°C to +150°C

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance, Junction to Case	1.52°C/W

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DC-0007552
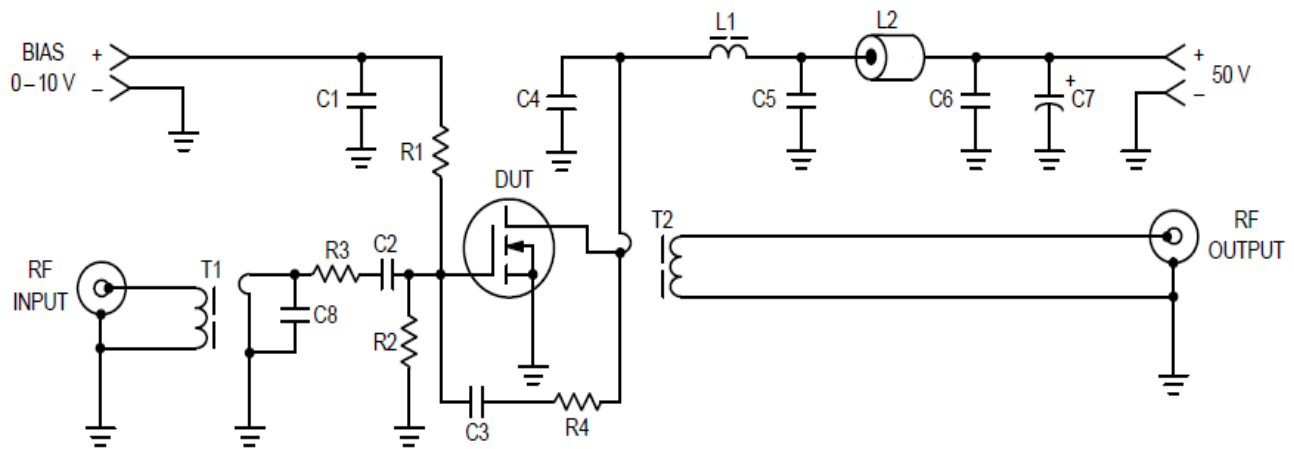
C1, C2, C3, C4, C5, C6 — 0.1 µF Ceramic Chip or Equivalent
C7 — 10 µF, 100 V Electrolytic
C8 — 100 pF Dipped Mica
L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 µH)
L2 — Ferrite Bead(s), 2.0 µH

R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 4.7 Ω, 1/2 W Carbon
R4 — 470 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:2 Impedance Transformer

Figure 1. 2.0 to 50 MHz Broadband Test Circuit
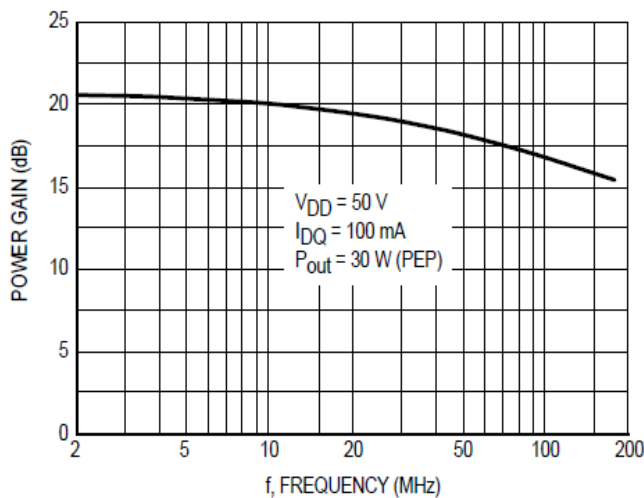
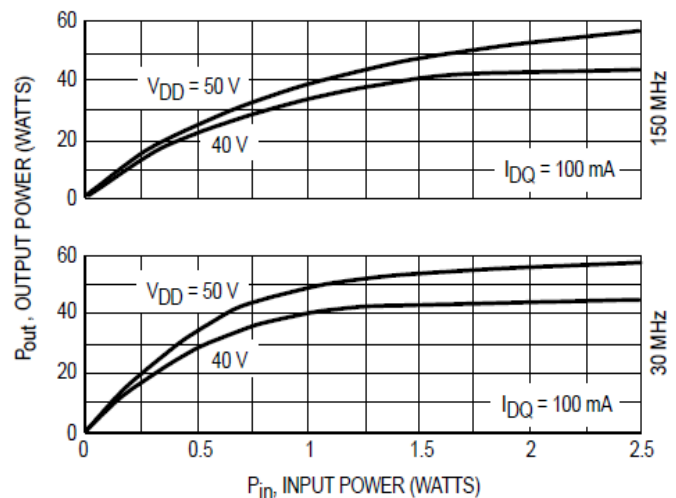**Figure 2. Power Gain versus Frequency**

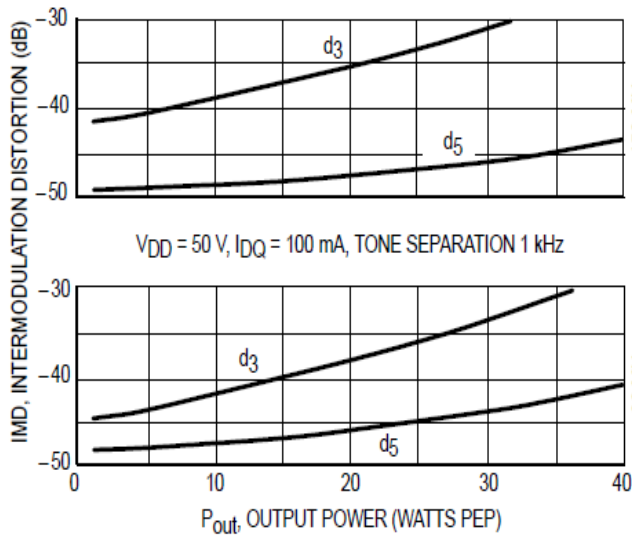**Figure 3. Output Power versus Input Power**

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DC-0007552

Figure 4. IMD versus P$_{out}$
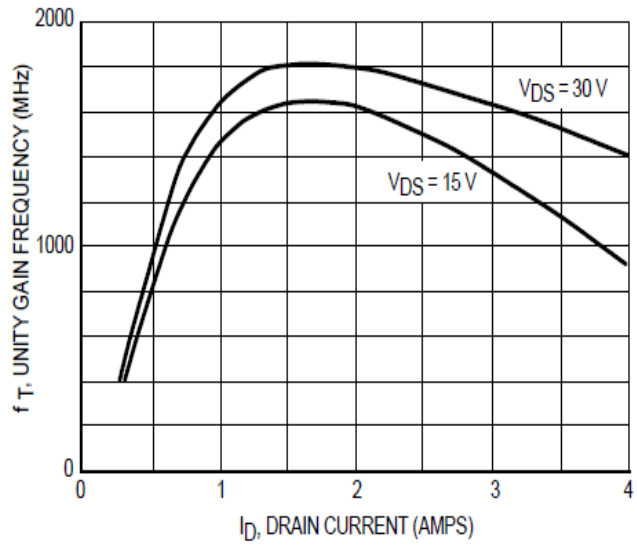
Figure 5. Common Source Unity Gain Frequency versus Drain Current

C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 µF Erie Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 µF, 50 Vdc Electrolytic
C6 — 15 pF Unelco Type J101
C7 — 24 pF Unelco Type MCM 01/010
L1 — 2 Turns #18 AWG, 5/16″ ID

L2 — 4 Turns #18 AWG, 5/16″ ID
R1 — 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75″ Subminiature
Coaxial Cable

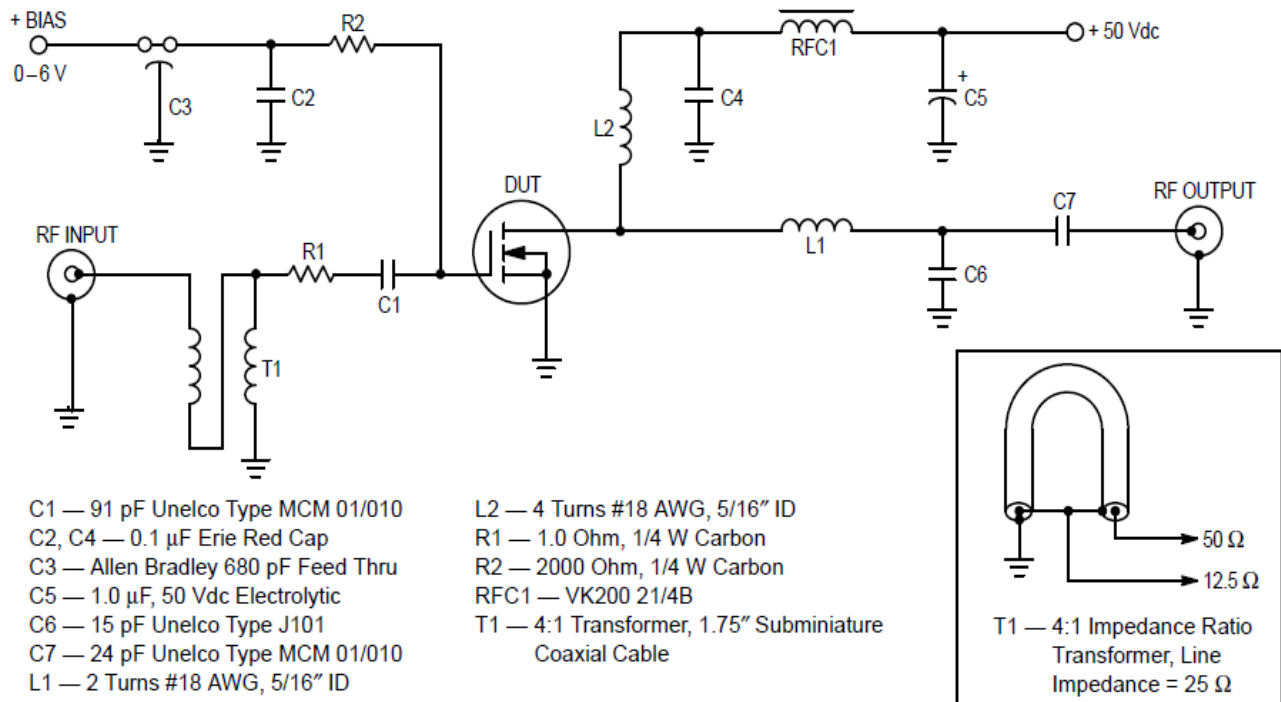T1 — 4:1 Impedance Ratio
Transformer, Line
Impedance = 25 Ω

Figure 6. 150 MHz Test Circuit
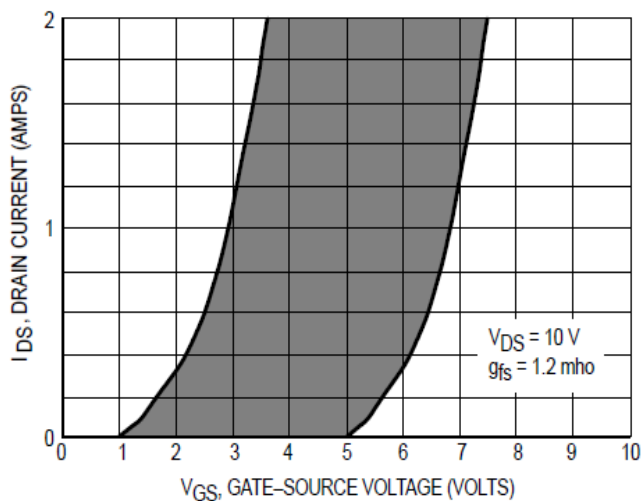
Figure 7. Gate Voltage versus Drain Current

$V_{DS} = 10\ V$
$g_{fs} = 1.2\ mho$

$T_C = 25°C$
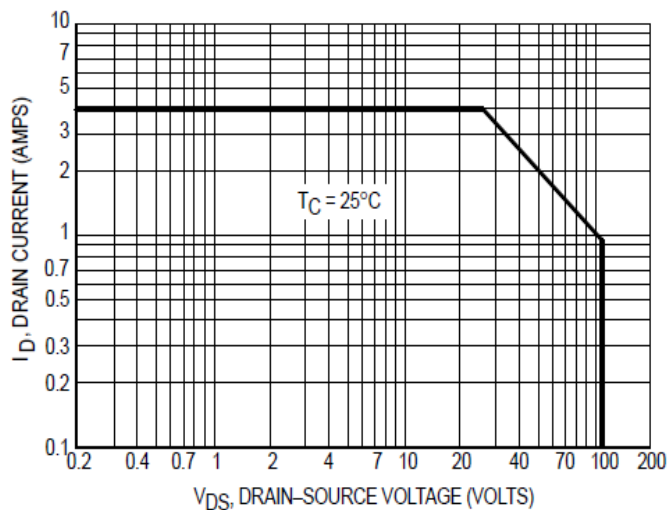
Figure 8. DC Safe Operating Area (SOA)
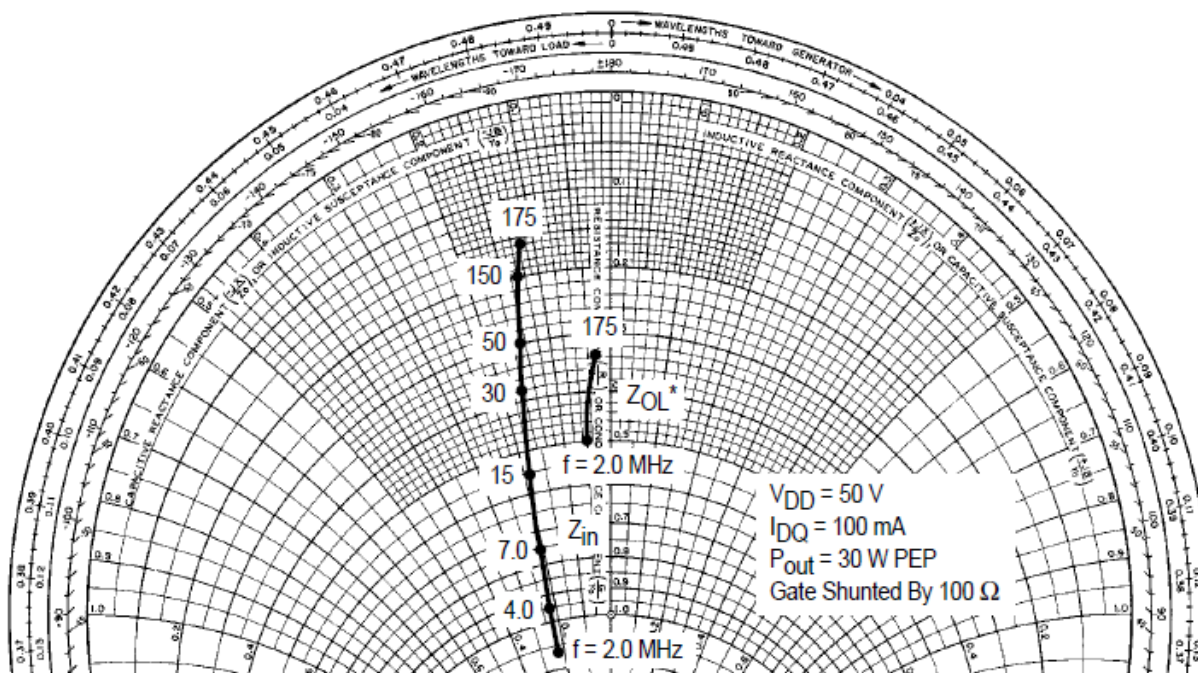

$V_{DD} = 50\ V$
$I_{DQ} = 100\ mA$
$P_{out} = 30\ W\ PEP$
Gate Shunted By 100 Ω

$Z_{OL}^* = $ Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

**Figure 9. Impedance Coordinates — 50 Ohm Characteristic Impedance**

RF Power MOSFET Considerations

MOSFET Capacitances

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (Cgd), and gate-to-source (Cgs). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (Cds).

These capacitances are characterized as input (Ciss), output (Coss), and reverse transfer (Crss) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The Ciss can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.

$$C_{iss} = C_{gd} + C_{gs}$$
$$C_{oss} = C_{gd} + C_{ds}$$
$$C_{rss} = C_{gd}$$
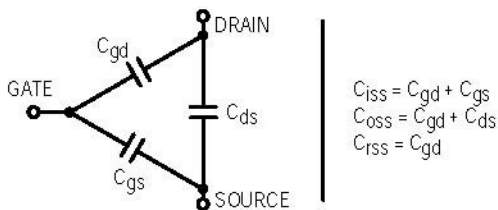
Linearity & Gain Characteristics

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to fT for bipolar transistors.

Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

Drain Characteristics

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, VDS(on), occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, VDS(on) has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

Gate Characteristics

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high on the order of 109 Ω resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, VGS(th).

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated VGS can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–cir-cuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}

$$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C} \qquad r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$$

Package Dimensions

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.370	0.390	9.40	9.90
C	0.229	0.281	5.82	7.13
D	0.215	0.235	5.47	5.96
E	0.085	0.105	2.16	2.66
H	0.150	0.108	3.81	4.57
J	0.004	0.006	0.11	0.15
K	0.395	0.405	10.04	10.28
M	40 °	50 °	40 °	50 °
Q	0.113	0.130	2.88	3.30
R	0.245	0.255	6.23	6.47
S	0.790	0.810	20.07	20.57
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211–07
ISSUE N

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