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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (March 2013) to Revision C | Page |
|--|-------------|
| <ul style="list-style-type: none"> Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Pin Configuration and Functions, Application and Implementation; Device and Documentation Support; Mechanical, Packaging, and Ordering Information | 1 |
| <ul style="list-style-type: none"> Changed "Junction Temperature Range" to "Operating Temperature Range" in Recommended Operating Conditions | 4 |
| <ul style="list-style-type: none"> Deleted $T_J = 25^\circ\text{C}$ in Electrical Characteristics tables | 5 |
| <ul style="list-style-type: none"> Deleted $T_J = 25^\circ\text{C}$ in Typical Performance Characteristics section | 11 |

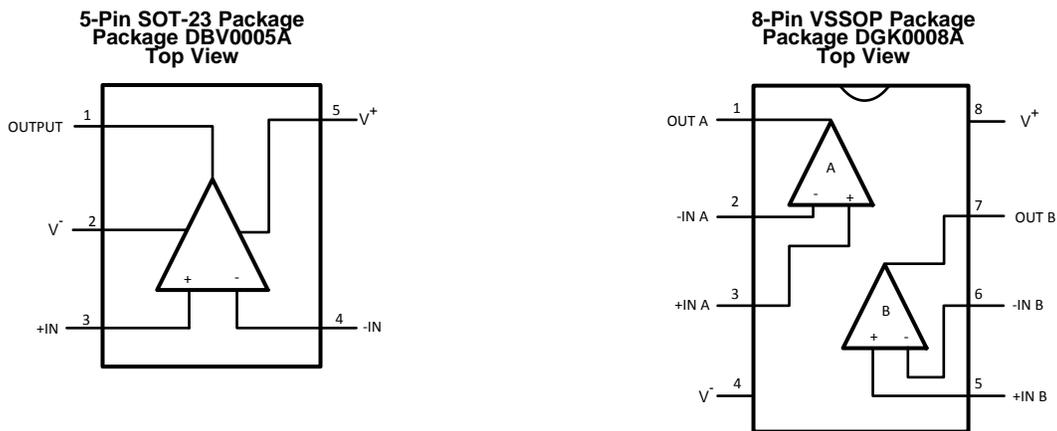
| Changes from Revision A (March 2013) to Revision B | Page |
|--|-------------|
| <ul style="list-style-type: none"> Changed layout of National Data Sheet to TI format | 24 |

5 Description (continued)

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12MHz under 150Ω load and $A_V = +2$) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in ADC buffer, and high frequency filter applications as well as other applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01°) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150Ω) and throughout the output voltage range. The LMH664X family is offered in single (LMH6642) and dual (LMH6643).

6 Pin Configuration and Functions



Pin Functions

| NAME | PIN NUMBER | | I/O | DESCRIPTION |
|----------------|------------|----------|-----|-------------------------|
| | LMH6642Q | LMH6643Q | | |
| -IN | 4 | | I | Inverting Input |
| +IN | 3 | | I | Non-inverting Input |
| -IN A | | 2 | I | ChA Inverting Input |
| +IN A | | 3 | I | ChA Non-inverting Input |
| -IN B | | 6 | I | ChB Inverting Input |
| +IN B | | 5 | I | ChB Non-inverting Input |
| OUT A | | 1 | O | ChA Output |
| OUT B | | 7 | O | ChB Output |
| OUTPUT | 1 | | O | Output |
| V ⁻ | 2 | 4 | I | Negative Supply |
| V ⁺ | 5 | 8 | I | Positive Supply |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|-----|--|------|
| V _{IN} Differential | | ±2.5 | V |
| Output Short Circuit Duration | | See ⁽³⁾ and ⁽⁴⁾ | |
| Supply Voltage (V ⁺ - V ⁻) | | 13.5 | V |
| Voltage at Input/Output pins | | V ⁺ +0.8 V ⁻ -0.8 | V |
| Input Current | | ±10 | mA |
| Junction Temperature ⁽⁵⁾ | | +150 | °C |
| Soldering Information | | | |
| Infrared or Convection Reflow (20 sec) | | 235 | °C |
| Wave Soldering Lead Temp.(10 sec) | | 260 | °C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (4) Output short circuit duration is infinite for V_S < 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5ms.
- (5) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A)/R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

7.2 Handling Ratings

| | | MIN | MAX | UNIT |
|--------------------|---------------------------|---|------|------|
| T _{stg} | Storage temperature range | -65 | +150 | °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | 2000 | V |
| | | Machine Model (MM) ⁽²⁾ | 200 | |
| | | Charged Device Model (CDM), per AEC Q100-011 | 1000 | |

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification, 1.5kΩ in series with 100pF.
- (2) Machine Model, 0Ω in series with 200pF.

7.3 Recommended Operating Conditions⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| Supply Voltage (V ⁺ - V ⁻) | 2.7 | 10 | V |
| Operating Temperature Range ⁽²⁾ | -40 | +85 | °C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A)/R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | DBV05A | DGK08A | UNIT |
|--|---------|---------|------|
| | 5 PINS | 8 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance ⁽²⁾ | 265°C/W | 235°C/W | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
- (2) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A)/R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

7.5 3V Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|---------------------|---------------------------------|---|--------------------|--------------------|-----------------------|------------------|
| BW | -3dB BW | $A_V = +1$, $V_{OUT} = 200mV_{PP}$ | 80 | 115 | | MHz |
| | | $A_V = +2, -1$, $V_{OUT} = 200mV_{PP}$ | | 46 | | |
| BW _{0.1dB} | 0.1dB Gain Flatness | $A_V = +2$, $R_L = 150\Omega$ to $V^+/2$, $R_L = 402\Omega$, $V_{OUT} = 200mV_{PP}$ | | 19 | | MHz |
| PBW | Full Power Bandwidth | $A_V = +1$, -1dB, $V_{OUT} = 1V_{PP}$ | | 40 | | MHz |
| e_n | Input-Referred Voltage Noise | $f = 100kHz$ | | 17 | | nV/\sqrt{Hz} |
| | | $f = 1kHz$ | | 48 | | |
| i_n | Input-Referred Current Noise | $f = 100kHz$ | | 0.90 | | pA/\sqrt{Hz} |
| | | $f = 1kHz$ | | 3.3 | | |
| THD | Total Harmonic Distortion | $f = 5MHz$, $V_O = 2V_{PP}$, $A_V = -1$, $R_L = 100\Omega$ to $V^+/2$ | | -48 | | dBc |
| DG | Differential Gain | $V_{CM} = 1V$, NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$ | | 0.17% | | |
| | | $R_L = 1k\Omega$ to $V^+/2$ | | 0.03% | | |
| DP | Differential Phase | $V_{CM} = 1V$, NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$ | | 0.05 | | deg |
| | | $R_L = 1k\Omega$ to $V^+/2$ | | 0.03 | | |
| CT Rej. | Cross-Talk Rejection | $f = 5MHz$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$ | | 47 | | dB |
| T_S | Settling Time | $V_O = 2V_{PP}$, $\pm 0.1\%$, 8pF Load, $V_S = 5V$ | | 68 | | ns |
| SR | Slew Rate ⁽³⁾ | $A_V = -1$, $V_I = 2V_{PP}$ | 90 | 120 | | V/ μs |
| V_{OS} | Input Offset Voltage | For LMH6642 | | ± 1 | ± 5 ± 7 | mV |
| | | For LMH6643 | | ± 1 | ± 3.4 ± 7 | |
| TC V_{OS} | Input Offset Average Drift | ⁽⁴⁾ | | ± 5 | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | ⁽⁵⁾ | | -1.50 | -2.60 -3.25 | μA |
| I_{OS} | Input Offset Current | | | 20 | 800 1000 | nA |
| R_{IN} | Common Mode Input Resistance | | | 3 | | M Ω |
| C_{IN} | Common Mode Input Capacitance | | | 2 | | pF |
| CMVR | Input Common-Mode Voltage Range | CMRR $\geq 50dB$ | | -0.5 | -0.2 -0.1 | V |
| | | | | 1.8 1.6 | 2.0 | |
| CMRR | Common Mode Rejection Ratio | V_{CM} Stepped from 0V to 1.5V | 72 | 95 | | dB |
| A_{VOL} | Large Signal Voltage Gain | $V_O = 0.5V$ to $2.5V$ $R_L = 2k\Omega$ to $V^+/2$ | 80 75 | 96 | | dB |
| | | $V_O = 0.5V$ to $2.5V$ $R_L = 150\Omega$ to $V^+/2$ | 74 70 | 82 | | |
| V_O | Output Swing High | $R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = 200mV$ | 2.90 | 2.98 | | V |
| | | $R_L = 150\Omega$ to $V^+/2$, $V_{ID} = 200mV$ | 2.80 | 2.93 | | |
| | Output Swing Low | $R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = -200mV$ | | 25 | 75 | mV |
| | | $R_L = 150\Omega$ to $V^+/2$, $V_{ID} = -200mV$ | | 75 | 150 | |

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.

(5) Positive current corresponds to current flowing into the device.

3V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|-----------|---------------------------------------|--|--------------------|--------------------|---------------------|------|
| I_{SC} | Output Short Circuit Current | Sourcing to $V^+/2$ $V_{ID} = 200mV$ ⁽⁶⁾ | 50 35 | 95 | | mA |
| | | Sinking to $V^+/2$ $V_{ID} = -200mV$ ⁽⁶⁾ | 55 40 | 110 | | |
| I_{OUT} | Output Current | $V_{OUT} = 0.5V$ from either supply | | ± 65 | | mA |
| +PSRR | Positive Power Supply Rejection Ratio | $V^+ = 3.0V$ to $3.5V$, $V_{CM} = 1.5V$ | 75 | 85 | | dB |
| I_S | Supply Current (per channel) | No Load | | 2.70 | 4.00 4.50 | mA |

(6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

7.6 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|---------------------|---------------------------------|---|--------------------|--------------------|--|------------------|
| BW | –3dB BW | $A_V = +1$, $V_{OUT} = 200mV_{PP}$ | 90 | 120 | | MHz |
| | | $A_V = +2$, -1 , $V_{OUT} = 200mV_{PP}$ | | 46 | | |
| BW _{0.1dB} | 0.1dB Gain Flatness | $A_V = +2$, $R_L = 150\Omega$ to $V^+/2$, $R_f = 402\Omega$, $V_{OUT} = 200mV_{PP}$ | | 15 | | MHz |
| PBW | Full Power Bandwidth | $A_V = +1$, $-1dB$, $V_{OUT} = 2V_{PP}$ | | 22 | | MHz |
| e_n | Input-Referred Voltage Noise | $f = 100kHz$ | | 17 | | nV/\sqrt{Hz} |
| | | $f = 1kHz$ | | 48 | | |
| i_n | Input-Referred Current Noise | $f = 100kHz$ | | 0.90 | | pA/\sqrt{Hz} |
| | | $f = 1kHz$ | | 3.3 | | |
| THD | Total Harmonic Distortion | $f = 5MHz$, $V_O = 2V_{PP}$, $A_V = +2$ | | –60 | | dBc |
| DG | Differential Gain | NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$ | | 0.16% | | |
| | | $R_L = 1k\Omega$ to $V^+/2$ | | 0.05% | | |
| DP | Differential Phase | NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$ | | 0.05 | | deg |
| | | $R_L = 1k\Omega$ to $V^+/2$ | | 0.01 | | |
| CT Rej. | Cross-Talk Rejection | $f = 5MHz$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$ | | 47 | | dB |
| T_S | Settling Time | $V_O = 2V_{PP}$, $\pm 0.1\%$, 8pF Load | | 68 | | ns |
| SR | Slew Rate ⁽³⁾ | $A_V = -1$, $V_I = 2V_{PP}$ | 95 | 125 | | V/ μs |
| V_{OS} | Input Offset Voltage | For LMH6642 | | ± 1 | ± 5 ± 7 | mV |
| | | For LMH6643 | | ± 1 | ± 3.4 ± 7 | |
| TC V_{OS} | Input Offset Average Drift | ⁽⁴⁾ | | ± 5 | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | ⁽⁵⁾ | | –1.70 | –2.60 –3.25 | μA |
| I_{OS} | Input Offset Current | | | 20 | 800 1000 | nA |
| R_{IN} | Common Mode Input Resistance | | | 3 | | M Ω |
| C_{IN} | Common Mode Input Capacitance | | | 2 | | pF |
| CMVR | Input Common-Mode Voltage Range | CMRR $\geq 50dB$ | | –0.5 | –0.2 –0.1 | V |
| | | | | 3.8 3.6 | 4.0 | |
| CMRR | Common Mode Rejection Ratio | V_{CM} Stepped from 0V to 3.5V | 72 | 95 | | dB |
| A_{VOL} | Large Signal Voltage Gain | $V_O = 0.5V$ to 4.50V $R_L = 2k\Omega$ to $V^+/2$ | 86 82 | 98 | | dB |
| | | $V_O = 0.5V$ to 4.25V $R_L = 150\Omega$ to $V^+/2$ | 76 72 | 82 | | |
| V_O | Output Swing High | $R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = 200mV$ | 4.90 | 4.98 | | V |
| | | $R_L = 150\Omega$ to $V^+/2$, $V_{ID} = 200mV$ | 4.65 | 4.90 | | |
| | Output Swing Low | $R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = -200mV$ | | 25 | 100 | mV |
| | | $R_L = 150\Omega$ to $V^+/2$, $V_{ID} = -200mV$ | | 100 | 150 | |

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.

(5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|-----------|---------------------------------------|--|--------------------|--------------------|---------------------|------|
| I_{SC} | Output Short Circuit Current | Sourcing to $V^+/2$ $V_{ID} = 200mV$ ⁽⁶⁾ | 55 40 | 115 | | mA |
| | | Sinking to $V^+/2$ $V_{ID} = -200mV$ ⁽⁶⁾ | 70 55 | 140 | | |
| I_{OUT} | Output Current | $V_O = 0.5V$ from either supply | | ± 70 | | mA |
| +PSRR | Positive Power Supply Rejection Ratio | $V^+ = 4.0V$ to $6V$ | 79 | 90 | | dB |
| I_S | Supply Current (per channel) | No Load | | 2.70 | 4.25 5.00 | mA |

(6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

7.7 ±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to ground. **Boldface** limits apply at the temperature extremes.

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|---------------------|---------------------------------|---|--------------------------|--------------------|--|------------------|
| BW | –3dB BW | $A_V = +1$, $V_{OUT} = 200mV_{PP}$ | 95 | 130 | | MHz |
| | | $A_V = +2$, -1 , $V_{OUT} = 200mV_{PP}$ | | 46 | | |
| BW _{0.1dB} | 0.1dB Gain Flatness | $A_V = +2$, $R_L = 150\Omega$ to $V^+/2$, $R_f = 806\Omega$, $V_{OUT} = 200mV_{PP}$ | | 12 | | MHz |
| PBW | Full Power Bandwidth | $A_V = +1$, $-1dB$, $V_{OUT} = 2V_{PP}$ | | 24 | | MHz |
| e_n | Input-Referred Voltage Noise | $f = 100kHz$ | | 17 | | nV/\sqrt{Hz} |
| | | $f = 1kHz$ | | 48 | | |
| i_n | Input-Referred Current Noise | $f = 100kHz$ | | 0.90 | | pA/\sqrt{Hz} |
| | | $f = 1kHz$ | | 3.3 | | |
| THD | Total Harmonic Distortion | $f = 5MHz$, $V_O = 2V_{PP}$, $A_V = +2$ | | –62 | | dBc |
| DG | Differential Gain | NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$ | | 0.15% | | |
| | | $R_L = 1k\Omega$ to $V^+/2$ | | 0.01% | | |
| DP | Differential Phase | NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$ | | 0.04 | | deg |
| | | $R_L = 1k\Omega$ to $V^+/2$ | | 0.01 | | |
| CT Rej. | Cross-Talk Rejection | $f = 5MHz$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$ | | 47 | | dB |
| T_S | Settling Time | $V_O = 2V_{PP}$, $\pm 0.1\%$, 8pF Load, $V_S = 5V$ | | 68 | | ns |
| SR | Slew Rate ⁽³⁾ | $A_V = -1$, $V_I = 2V_{PP}$ | 100 | 135 | | V/ μ s |
| V_{OS} | Input Offset Voltage | For LMH6642 | | ± 1 | ± 5 ± 7 | mV |
| | | For LMH6643 | | ± 1 | ± 3.4 ± 7 | |
| TC V_{OS} | Input Offset Average Drift | ⁽⁴⁾ | | ± 5 | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | ⁽⁵⁾ | | –1.60 | –2.60 –3.25 | μA |
| I_{OS} | Input Offset Current | | | 20 | 800 1000 | nA |
| R_{IN} | Common Mode Input Resistance | | | 3 | | M Ω |
| C_{IN} | Common Mode Input Capacitance | | | 2 | | pF |
| CMVR | Input Common-Mode Voltage Range | CMRR $\geq 50dB$ | | –5.5 | –5.2 –5.1 | V |
| | | | 3.8 3.6 | 4.0 | | |
| CMRR | Common Mode Rejection Ratio | V_{CM} Stepped from $-5V$ to $3.5V$ | 74 | 95 | | dB |
| A_{VOL} | Large Signal Voltage Gain | $V_O = -4.5V$ to $4.5V$, $R_L = 2k\Omega$ | 88 84 | 96 | | dB |
| | | $V_O = -4.0V$ to $4.0V$, $R_L = 150\Omega$ | 78 74 | 82 | | |
| V_O | Output Swing High | $R_L = 2k\Omega$, $V_{ID} = 200mV$ | 4.90 | 4.96 | | V |
| | | $R_L = 150\Omega$, $V_{ID} = 200mV$ | 4.65 | 4.80 | | |
| | Output Swing Low | $R_L = 2k\Omega$, $V_{ID} = -200mV$ | | –4.96 | –4.90 | V |
| | | $R_L = 150\Omega$, $V_{ID} = -200mV$ | | –4.80 | –4.65 | |

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.

(5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$, V_{ID} (input differential voltage) as noted (where applicable) and $R_L = 2k\Omega$ to ground. **Boldface** limits apply at the temperature extremes.

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|-----------|------------------------------|---|--------------------|--------------------|---------------------|------|
| I_{SC} | Output Short Circuit Current | Sourcing to Ground $V_{ID} = 200mV$ ⁽⁶⁾ | 60 35 | 115 | | mA |
| | | Sinking to Ground $V_{ID} = -200mV$ ⁽⁶⁾ | 85 65 | 145 | | |
| I_{OUT} | Output Current | $V_O = 0.5V$ from either supply | ± 75 | | | mA |
| PSRR | Power Supply Rejection Ratio | $(V^+, V^-) = (4.5V, -4.5V)$ to $(5.5V, -5.5V)$ | 78 | 90 | | dB |
| I_S | Supply Current (per channel) | No Load | | 2.70 | 4.50 5.50 | mA |

(6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

7.8 Typical Performance Characteristics

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

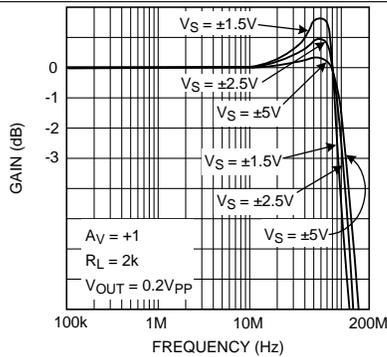


Figure 1. Closed Loop Frequency Response for Various Supplies

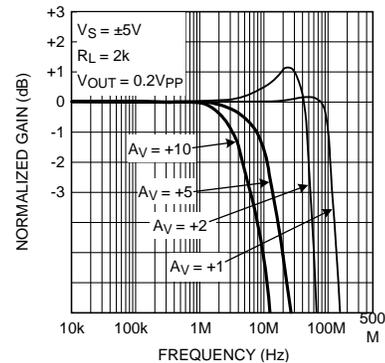


Figure 2. Closed Loop Gain vs. Frequency for Various Gain

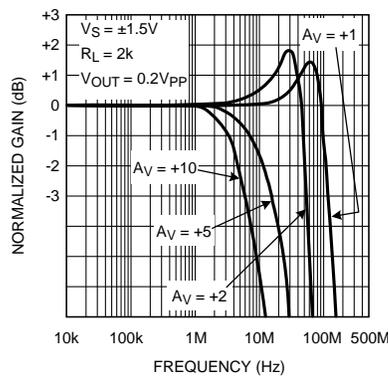


Figure 3. Closed Loop Gain vs. Frequency for Various Gain

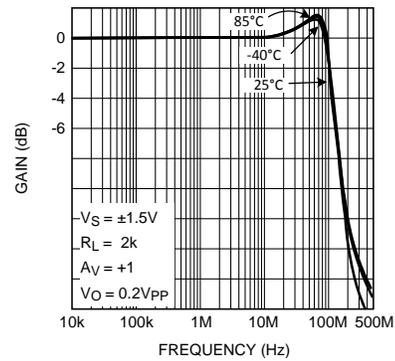


Figure 4. Closed Loop Frequency Response for Various Temperature

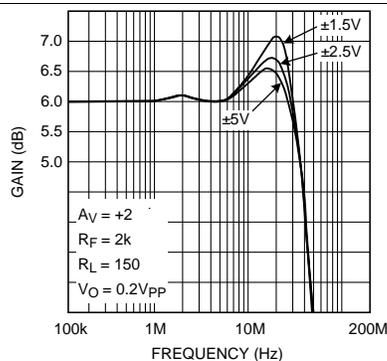


Figure 5. Closed Loop Gain vs. Frequency for Various Supplies

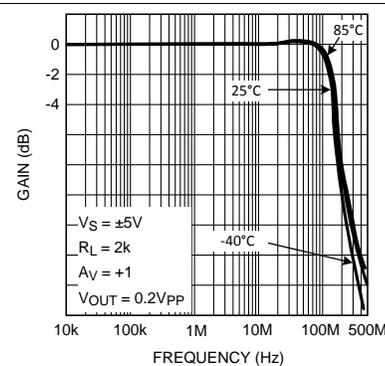


Figure 6. Closed Loop Frequency Response for Various Temperature

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

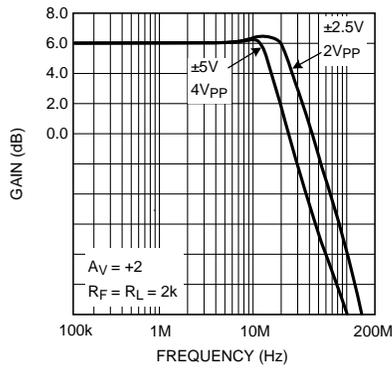


Figure 7. Large Signal Frequency Response

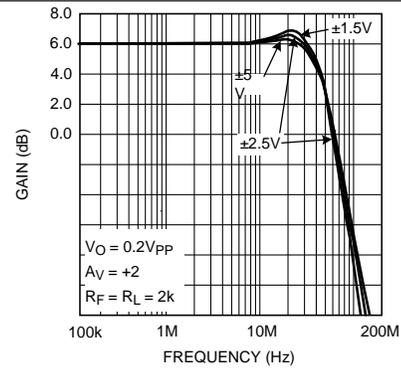


Figure 8. Closed Loop Small Signal Frequency Response for Various Supplies

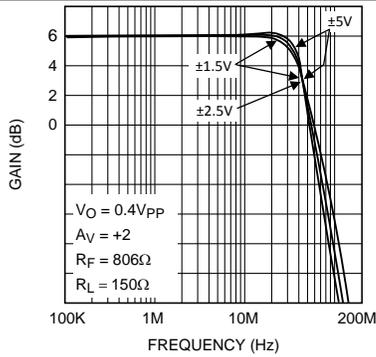


Figure 9. Closed Loop Frequency Response for Various Supplies

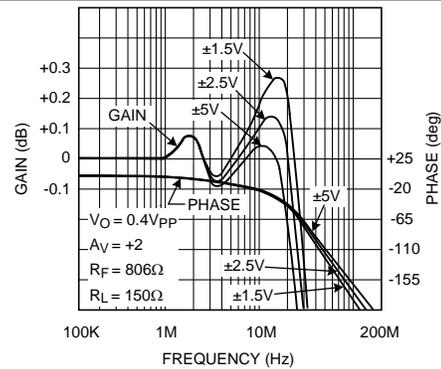


Figure 10. ±0.1dB Gain Flatness for Various Supplies

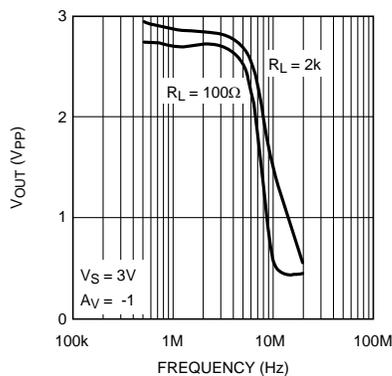


Figure 11. V_{OUT} (Vpp) for THD < 0.5%

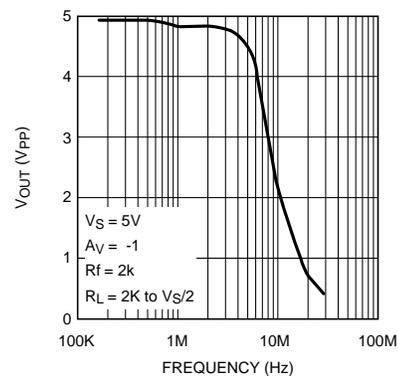


Figure 12. V_{OUT} (Vpp) for THD < 0.5%

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

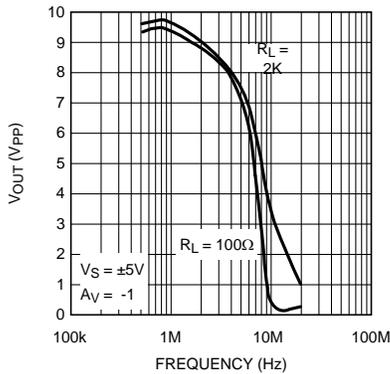


Figure 13. V_{OUT} (V_{PP}) for THD < 0.5%

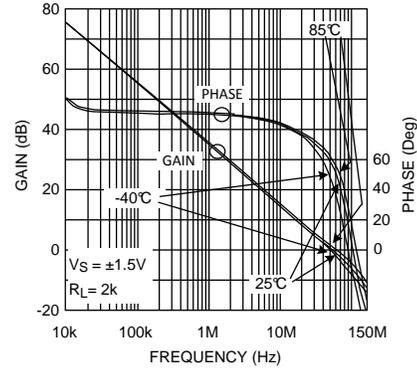


Figure 14. Open Loop Gain/Phase for Various Temperature

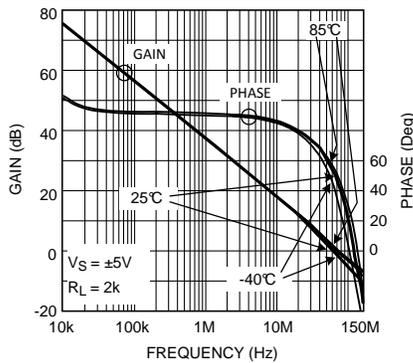


Figure 15. Open Loop Gain/Phase for Various Temperature

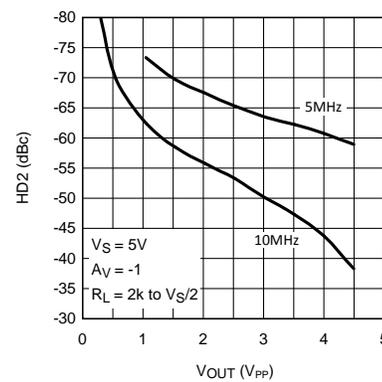


Figure 16. HD2 (dBc) vs. Output Swing

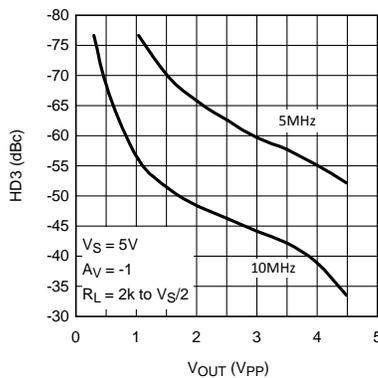


Figure 17. HD3 (dBc) vs. Output Swing

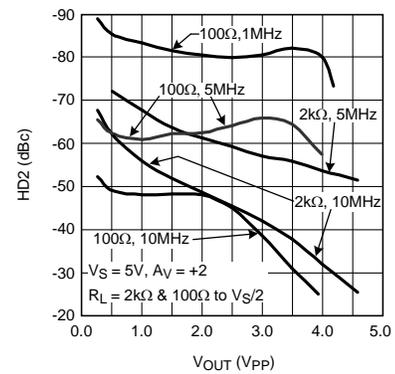


Figure 18. HD2 vs. Output Swing

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

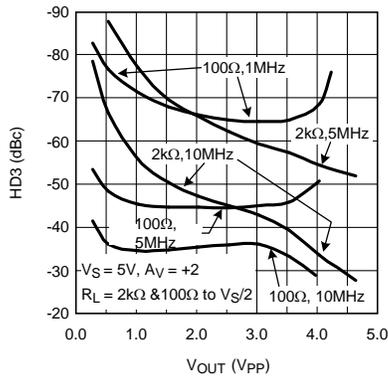


Figure 19. HD3 vs. Output Swing

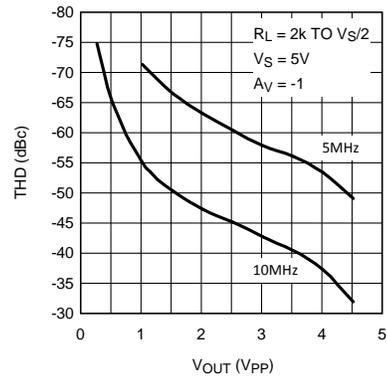


Figure 20. THD (dBc) vs. Output Swing

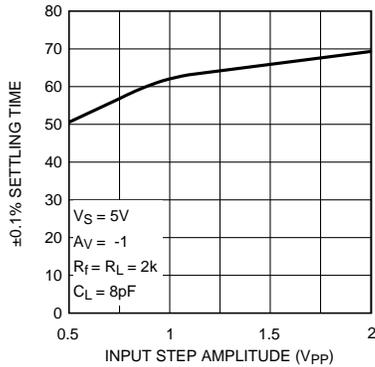


Figure 21. Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)

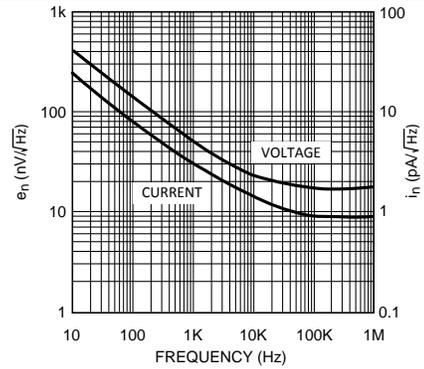


Figure 22. Input Noise vs. Frequency

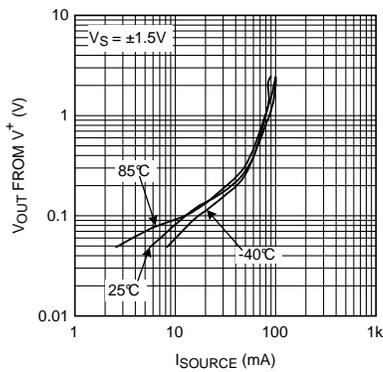


Figure 23. V_{OUT} from V^+ vs. I_{SOURCE}

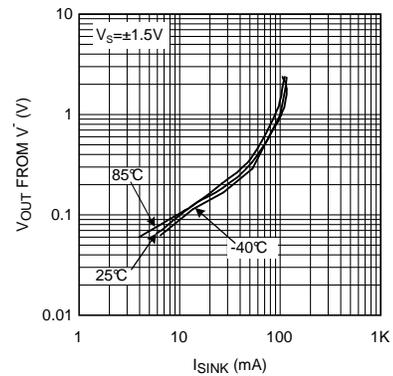


Figure 24. V_{OUT} from V^- vs. I_{SINK}

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

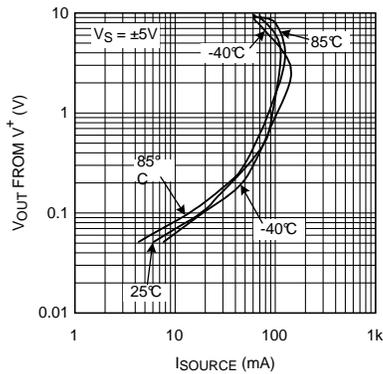


Figure 25. V_{OUT} from V^+ vs. I_{SOURCE}

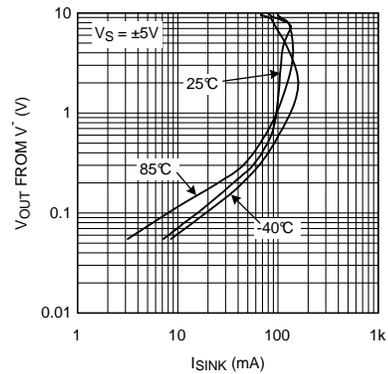


Figure 26. V_{OUT} from V^- vs. I_{SINK}

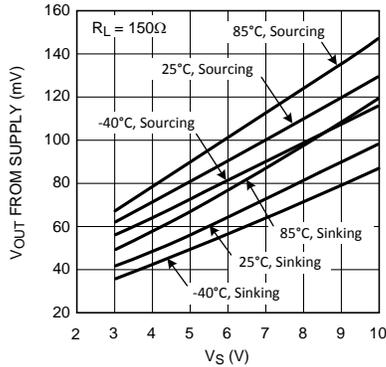


Figure 27. Swing vs. V_S

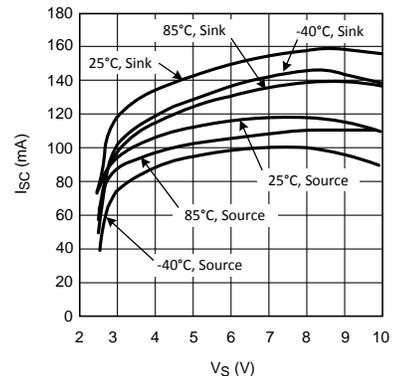


Figure 28. Short Circuit Current (to $V_S/2$) vs. V_S

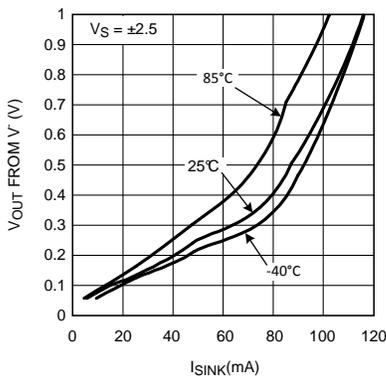


Figure 29. Output Sinking Saturation Voltage vs. I_{OUT}

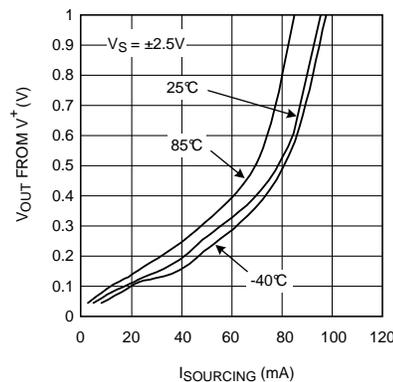


Figure 30. Output Sourcing Saturation Voltage vs. I_{OUT}

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

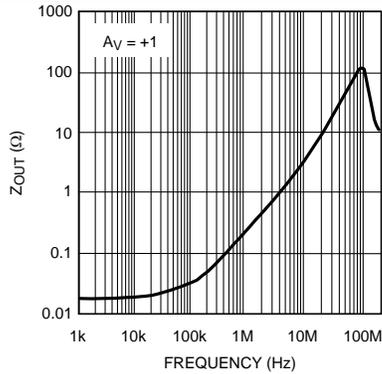


Figure 31. Closed Loop Output Impedance vs. Frequency, $A_V = +1$

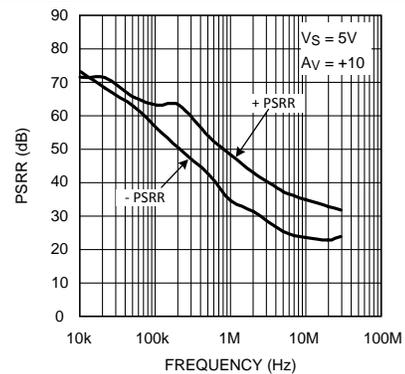


Figure 32. PSRR vs. Frequency

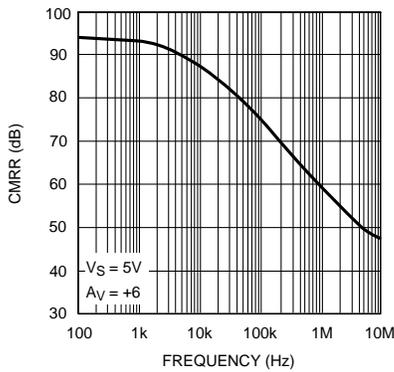


Figure 33. CMRR vs. Frequency

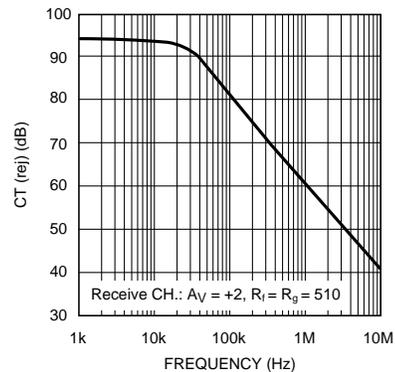


Figure 34. Crosstalk Rejection vs. Frequency (Output to Output)

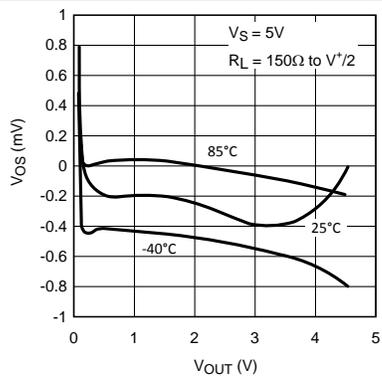


Figure 35. V_{OS} vs. V_{OUT} (Typical Unit)

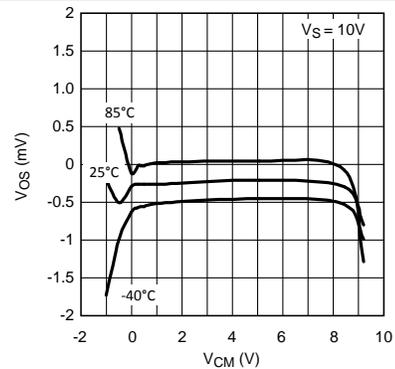


Figure 36. V_{OS} vs. V_{CM} (Typical Unit)

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

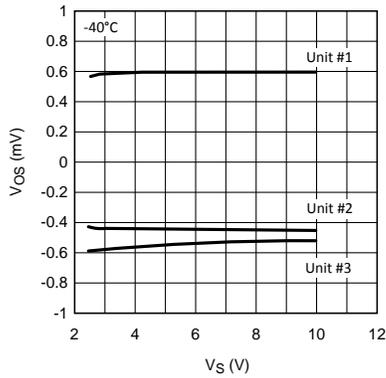


Figure 37. V_{OS} vs. V_S (for 3 Representative Units)

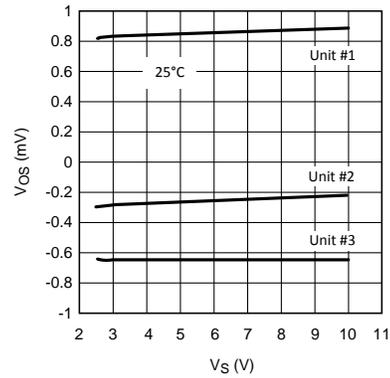


Figure 38. V_{OS} vs. V_S (for 3 Representative Units)

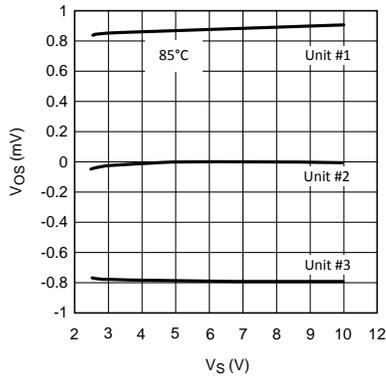


Figure 39. V_{OS} vs. V_S (for 3 Representative Units)

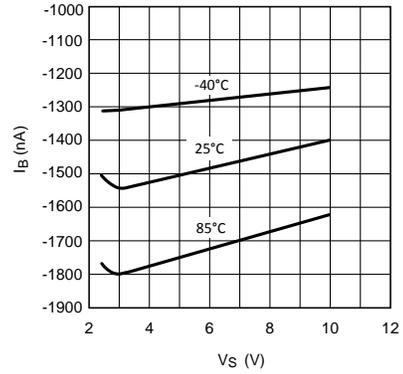


Figure 40. I_B vs. V_S

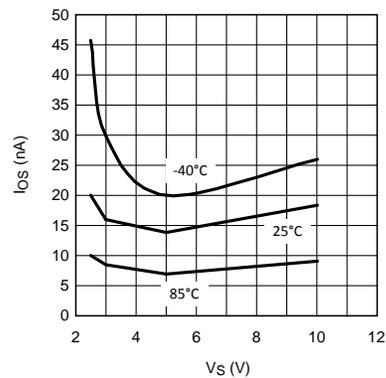


Figure 41. I_{OS} vs. V_S

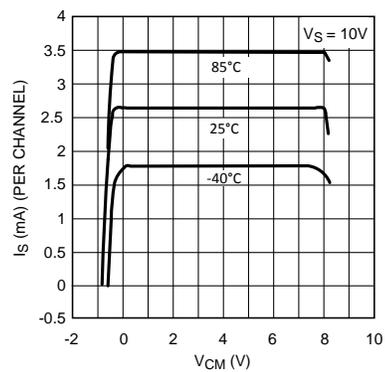
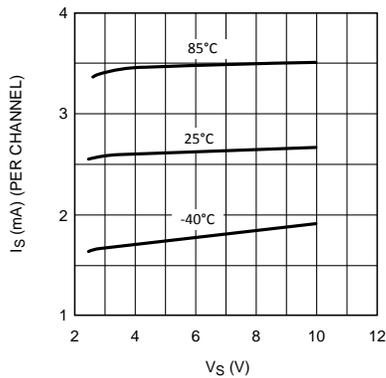
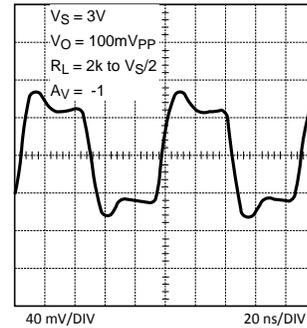
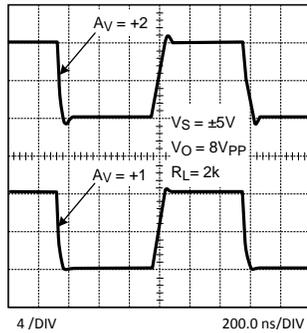
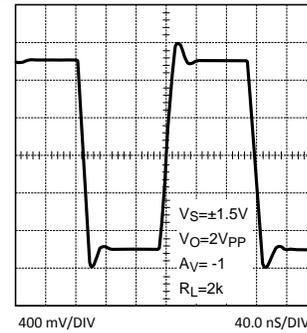
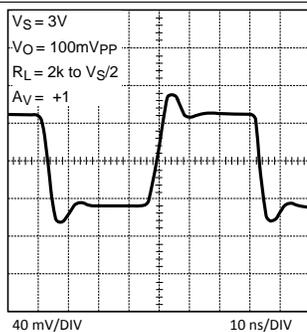
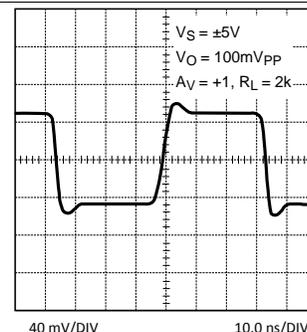


Figure 42. I_S vs. V_{CM}

Typical Performance Characteristics (continued)
 $V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

Figure 43. I_S vs. V_S

Figure 44. Small Signal Step Response

Figure 45. Large Signal Step Response

Figure 46. Large Signal Step Response

Figure 47. Small Signal Step Response

Figure 48. Small Signal Step Response

Typical Performance Characteristics (continued)

$V^+ = +5V$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

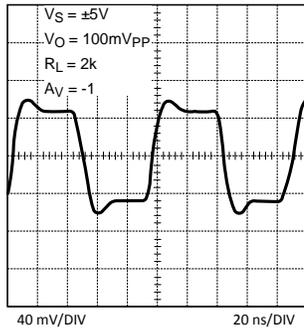


Figure 49. Small Signal Step Response

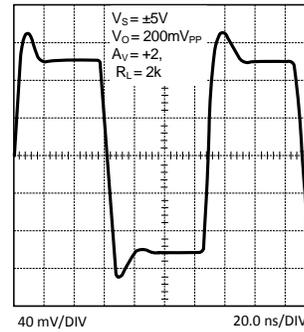


Figure 50. Small Signal Step Response

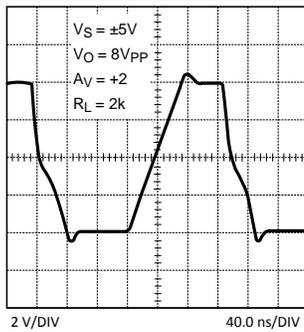


Figure 51. Large Signal Step Response

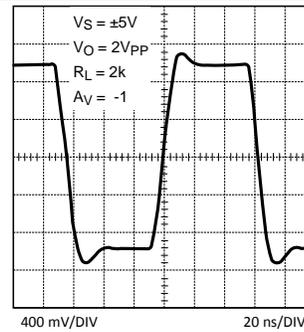


Figure 52. Large Signal Step Response

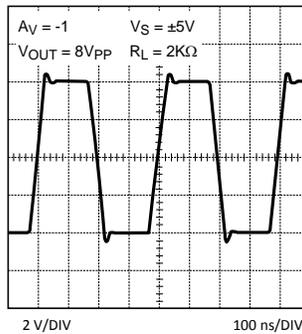


Figure 53. Large Signal Step Response

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Circuit Description

The LMH664X family is based on Texas Instruments' proprietary VIP10 dielectrically isolated bipolar process.

This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7 V) and low bias current.
- A class A-B “turn-around” stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75mA output current (at 0.5V from the supply rails) while consuming only 2.7 mA of total supply current per channel. This architecture allows output to reach within milli-volts of either supply rail.
- Consistent performance over the entire operating supply voltage range with little variation for the most important specifications (for example, BW, SR, I_{OUT} , and so forth).
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

8.1.1 Application Hints

This Op Amp family is a drop-in replacement for the AD805X family of high speed Op Amps in most applications. In addition, the LMH664X will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family's ensured parameters are included in the list of LMH664X ensured specifications in order to ensure equal or better level of performance. However, as in most high performance parts, due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

With 3V supplies and a common mode input voltage range that extends 0.5V below V^- , the LMH664X find applications in low voltage/low power applications. Even with 3V supplies, the -3dB BW (@ $A_V = +1$) is typically 115MHz with a tested limit of 80MHz. Production testing ensures that process variations with not compromise speed. High frequency response is exceptionally stable confining the typical -3dB BW over the industrial temperature range to $\pm 2.5\%$.

As can be seen from the [Typical Performance Characteristics](#), the LMH664X output current capability (~75mA) is enhanced compared to AD805X. This enhancement, increases the output load range, adding to the LMH664X's versatility.

Because of the LMH664X's high output current capability attention should be given to device junction temperature in order not to exceed the Absolute Maximum Rating.

Circuit Description (continued)

This device family was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See [Figure 54](#):

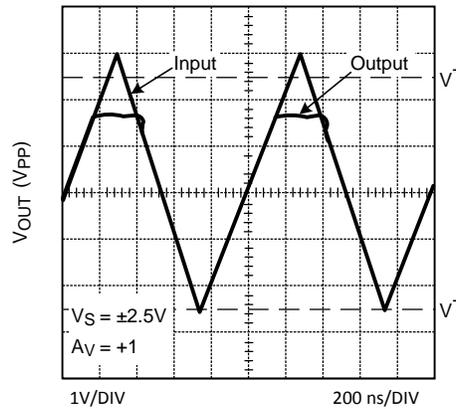


Figure 54. Input and Output Shown with CMVR Exceeded

However, if the input voltage range of $-0.5V$ to $1V$ from V^+ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct. The current in the diodes should be kept at or below $10mA$.

Output overdrive recovery time is less than $100ns$ as can be seen from [Figure 55](#) plot:

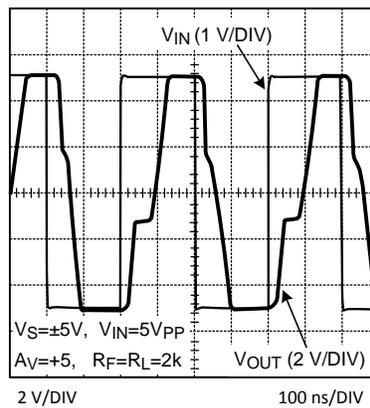


Figure 55. Overload Recovery Waveform

Circuit Description (continued)

8.1.2 Input and Output Topology

All input / output pins are protected against excessive voltages by ESD diodes connected to V^+ and V^- rails (see [Figure 56](#)). These diodes start conducting when the input / output pin voltage approaches $1V_{be}$ beyond V^+ or V^- to protect against over voltage. These diodes are normally reverse biased. Further protection of the inputs is provided by the two resistors (R in [Figure 56](#)), in conjunction with the string of anti-parallel diodes connected between both bases of the input stage. The combination of these resistors and diodes reduces excessive differential input voltages approaching $2V_{be}$. The most common situation when this occurs is when the device is used as a comparator (or with little or no feedback) and the device inputs no longer follow each other. In such a case, the diodes may conduct. As a consequence, input current increases and the differential input voltage is clamped. It is important to make sure that the subsequent current flow through the device input pins does not violate the Absolute Maximum Ratings of the device. To limit the current through this protection circuit, extra series resistors can be placed. Together with the built-in series resistors of several hundred ohms, these external resistors can limit the input current to a safe number (i.e. $< 10\text{mA}$). Be aware that these input series resistors may impact the switching speed of the device and could slow down the device.

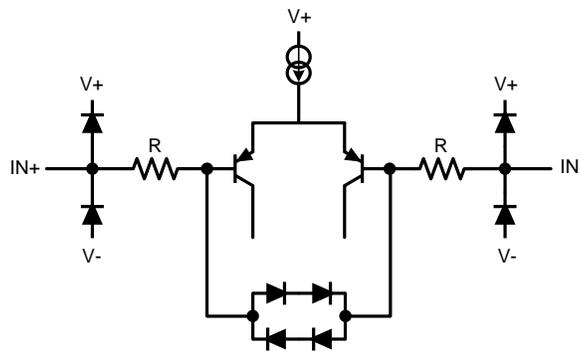


Figure 56. Input Equivalent Circuit

8.2 Single Supply, Low Power Photodiode Amplifier

The circuit shown in [Figure 57](#) is used to amplify the current from a photo-diode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664X family lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to 1mA_{pp} from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC}. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counteracting the effect of the C_{IN} and acting to stabilize the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin.

$$C_F = \sim \text{SQRT} \left[\frac{C_{IN}}{(2\pi \cdot \text{GBWP} \cdot R_F)} \right]$$

where GBWP is the Gain Bandwidth Product of the Op Amp (1)

Optimized as such, the I-V converter will have a theoretical pole, f_p, at:

$$f_p = \text{SQRT} \left[\frac{\text{GBWP}}{(2\pi R_F \cdot C_{IN})} \right] \quad (2)$$

With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, C_{IN} = 6pF. From [Typical Performance Characteristics](#), LMH6642/6643 family GBWP is approximately 57 MHz. Therefore, with R_f = 1k, from [Equation 1](#) and [Equation 2](#) above.

C_f = ~4.1 pF, and f_p = 39 MHz

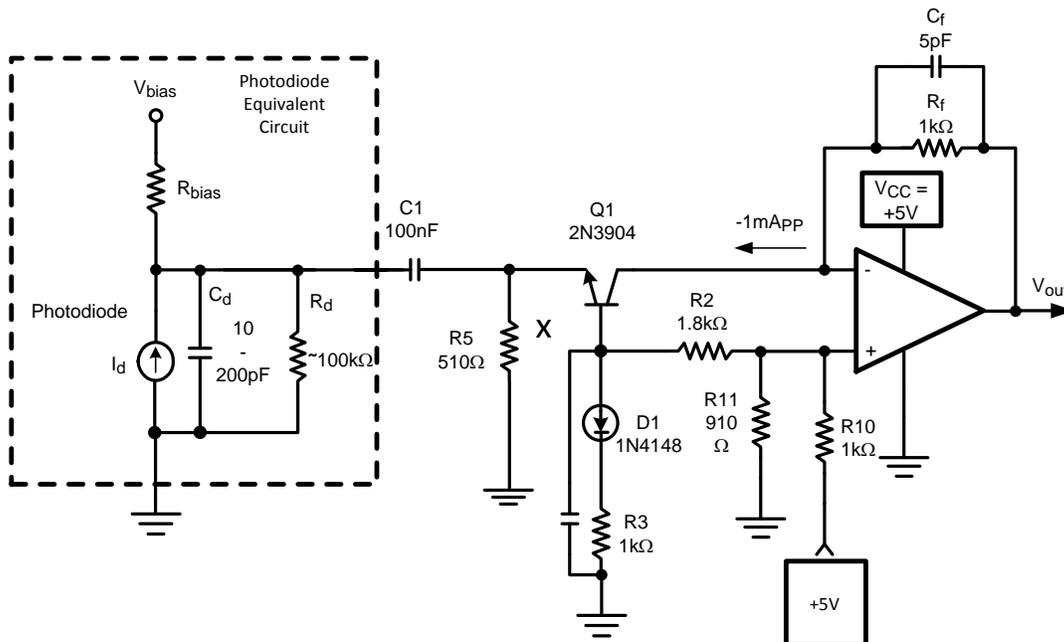


Figure 57. Single Supply Photodiode I-V Converter

Single Supply, Low Power Photodiode Amplifier (continued)

For this example, optimum C_f was empirically determined to be around 5pF. This time domain response is shown in [Figure 58](#) below showing about 9 ns rise/fall times, corresponding to about 39 MHz for f_p . The overall supply current from the +5 V supply is around 5 mA with no load.

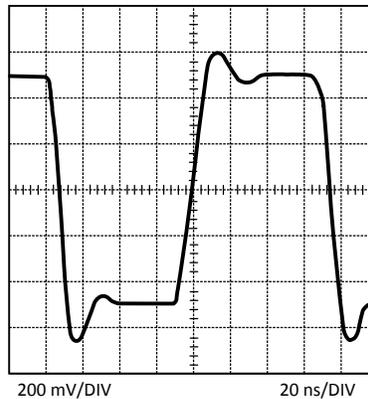


Figure 58. Converter Step Response (1V_{pp}, 20 ns/DIV)

8.3 Printed Circuit Board Layout and Component Values Section

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 ([SNOA367](#)) for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

| DEVICE | PACKAGE | EVALUATION BOARD PN |
|------------|--------------|---------------------|
| LMH6642QMF | 5-Pin SOT-23 | LMH730216 |
| LMH6643QMM | 8-Pin VSSOP | LMH730123 |

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| LMH6642Q-Q1 | Click here |
| LMH6643Q-Q1 | Click here |

9.3 Trademarks

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMH6642QMF/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | A64Q | Samples |
| LMH6642QMF/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | A64Q | Samples |
| LMH6643QMM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | 643Q | Samples |
| LMH6643QMM/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | 643Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

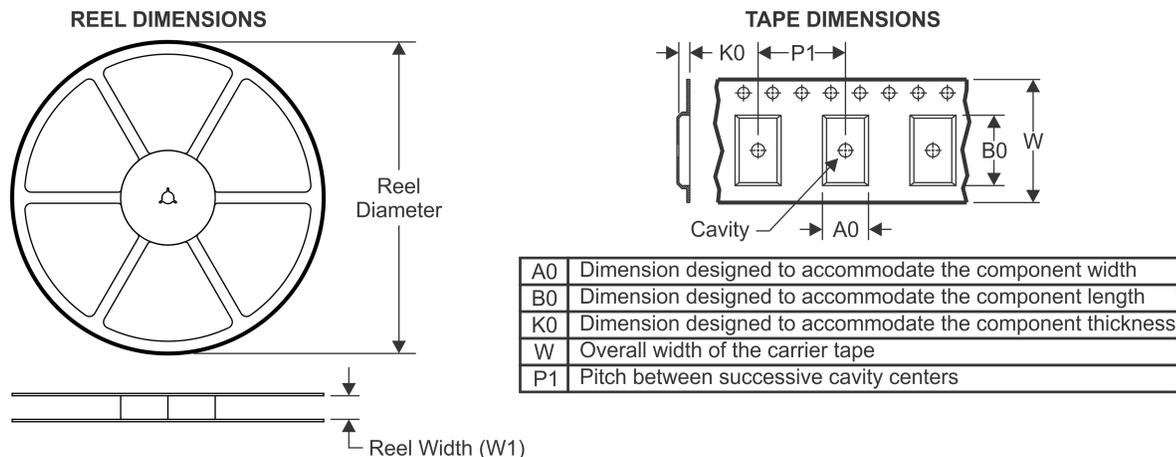
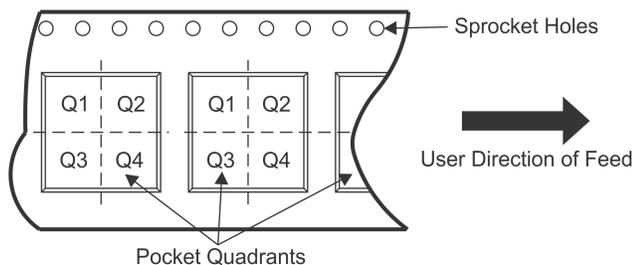
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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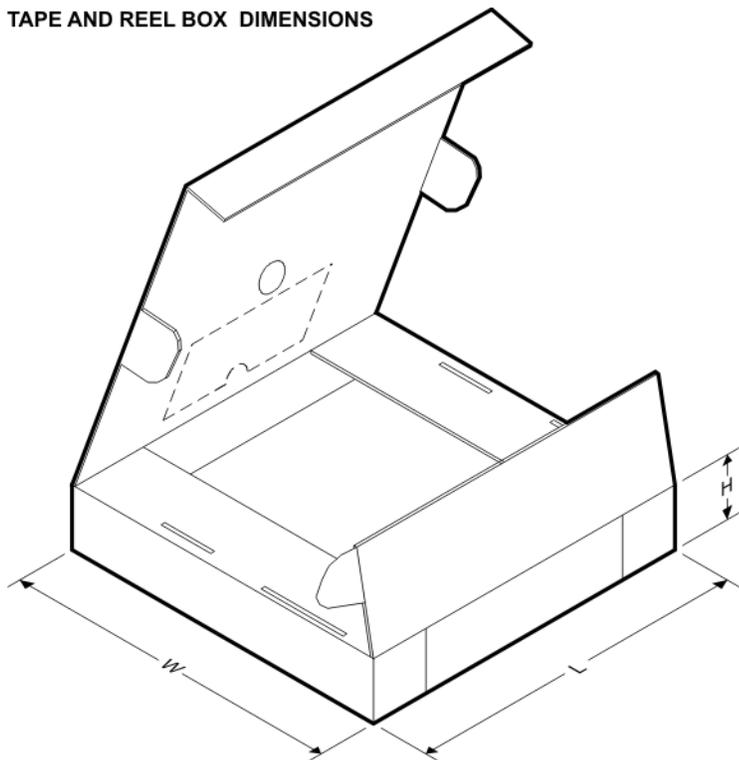
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMH6642QMF/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMH6642QMF/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMH6643QMM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMH6643QMM/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMH6642QMF/NOPB | SOT-23 | DBV | 5 | 1000 | 208.0 | 191.0 | 35.0 |
| LMH6642QMFX/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LMH6643QMM/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMH6643QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |

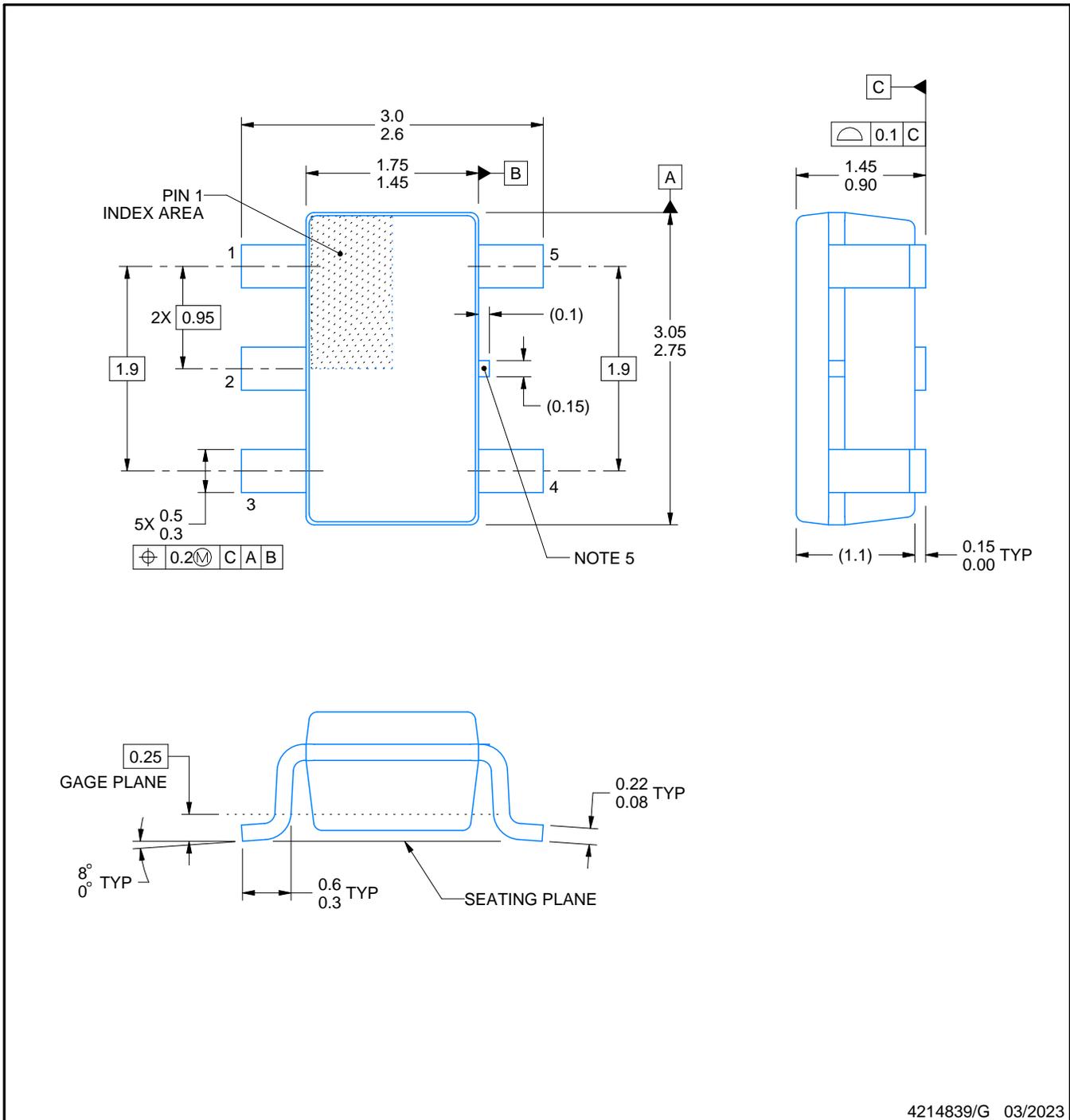
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

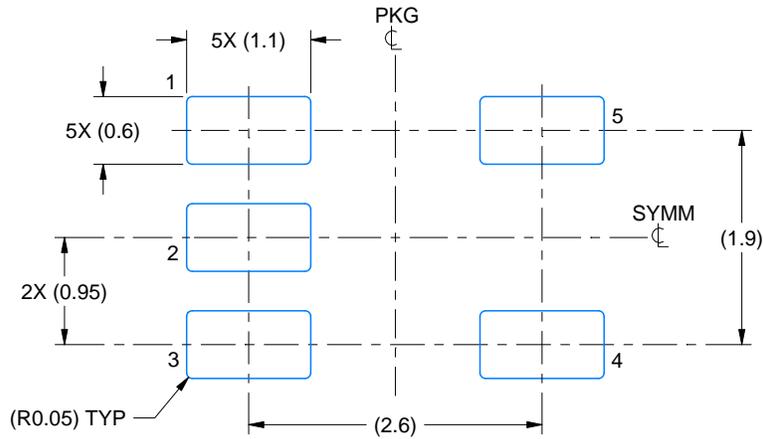
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

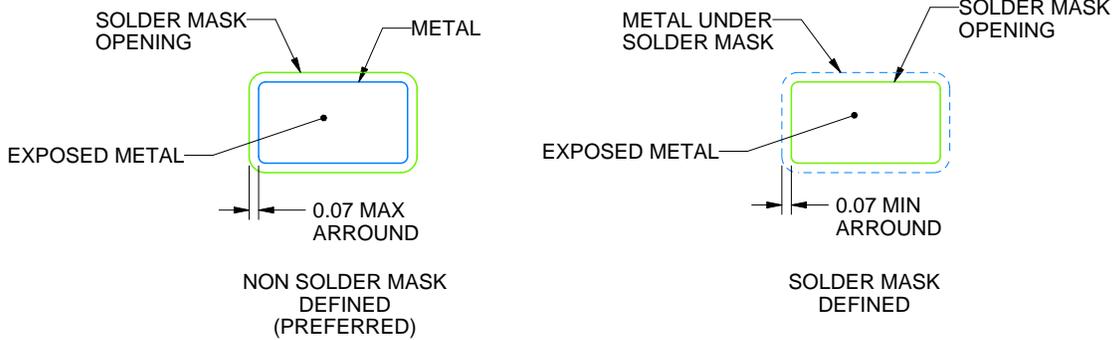
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

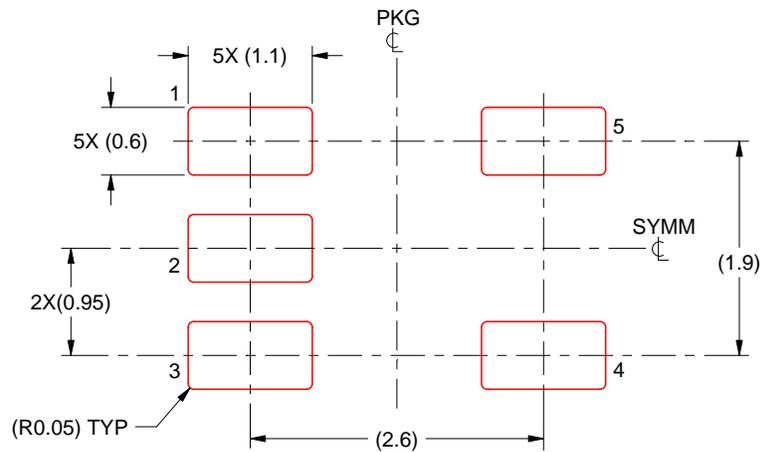
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

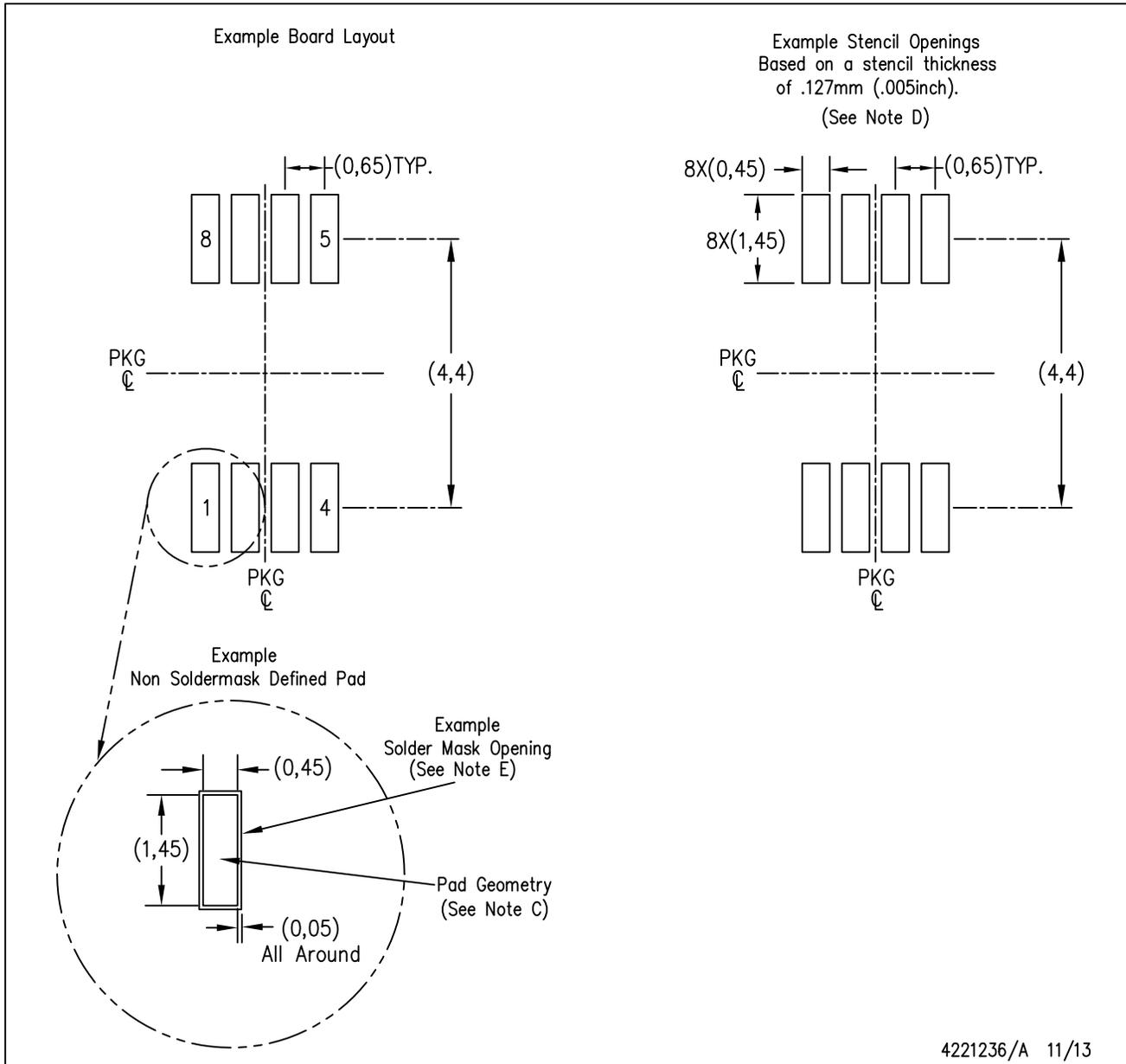


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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